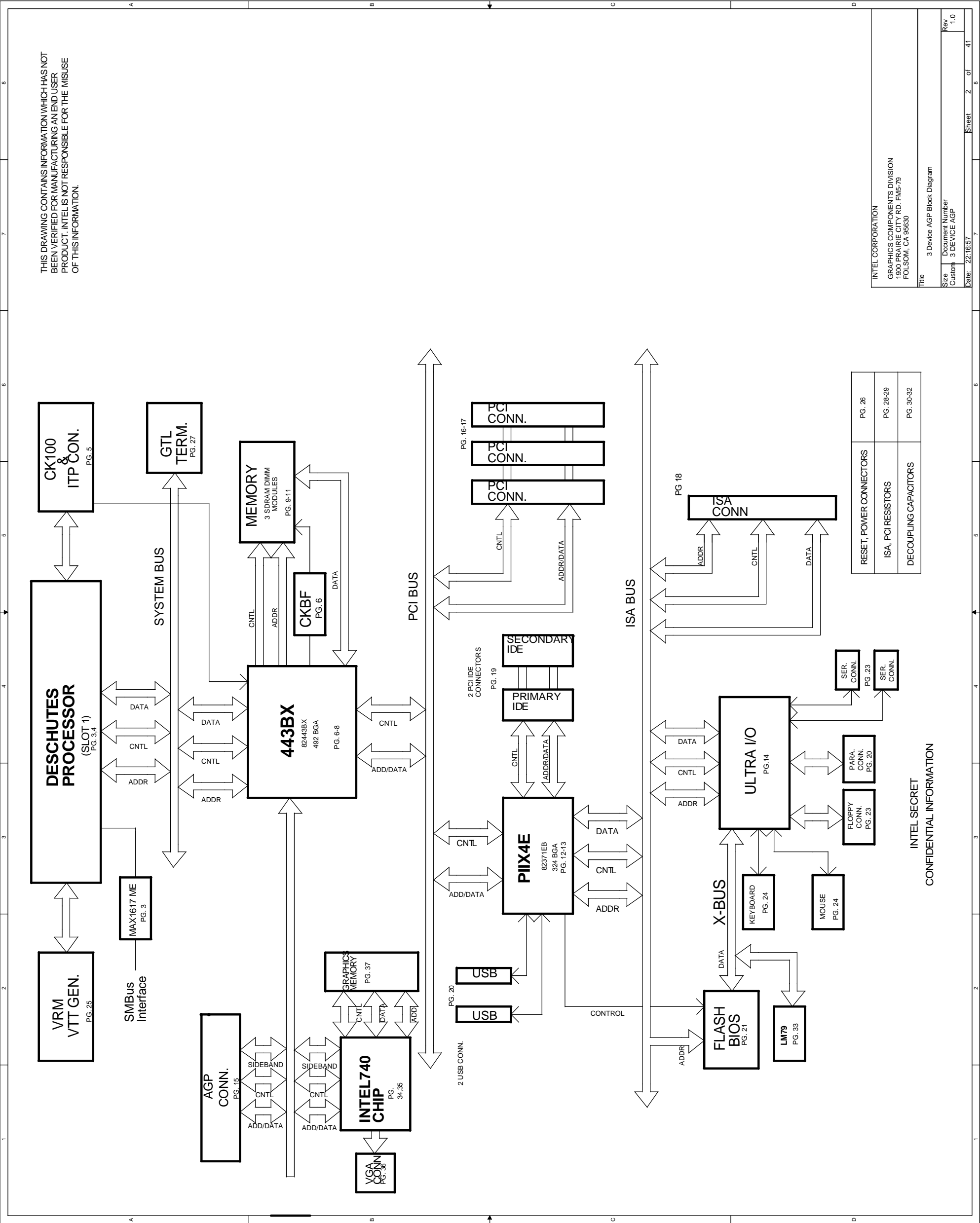


A			B		C		D		E		
4			3		2		1				
4			3		2		1				
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<div>Revision 1.0</div> <div>** Please note that these schematics are subject to change.</div>											
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Size										Document Number	
A										3 DEVICE AGP	
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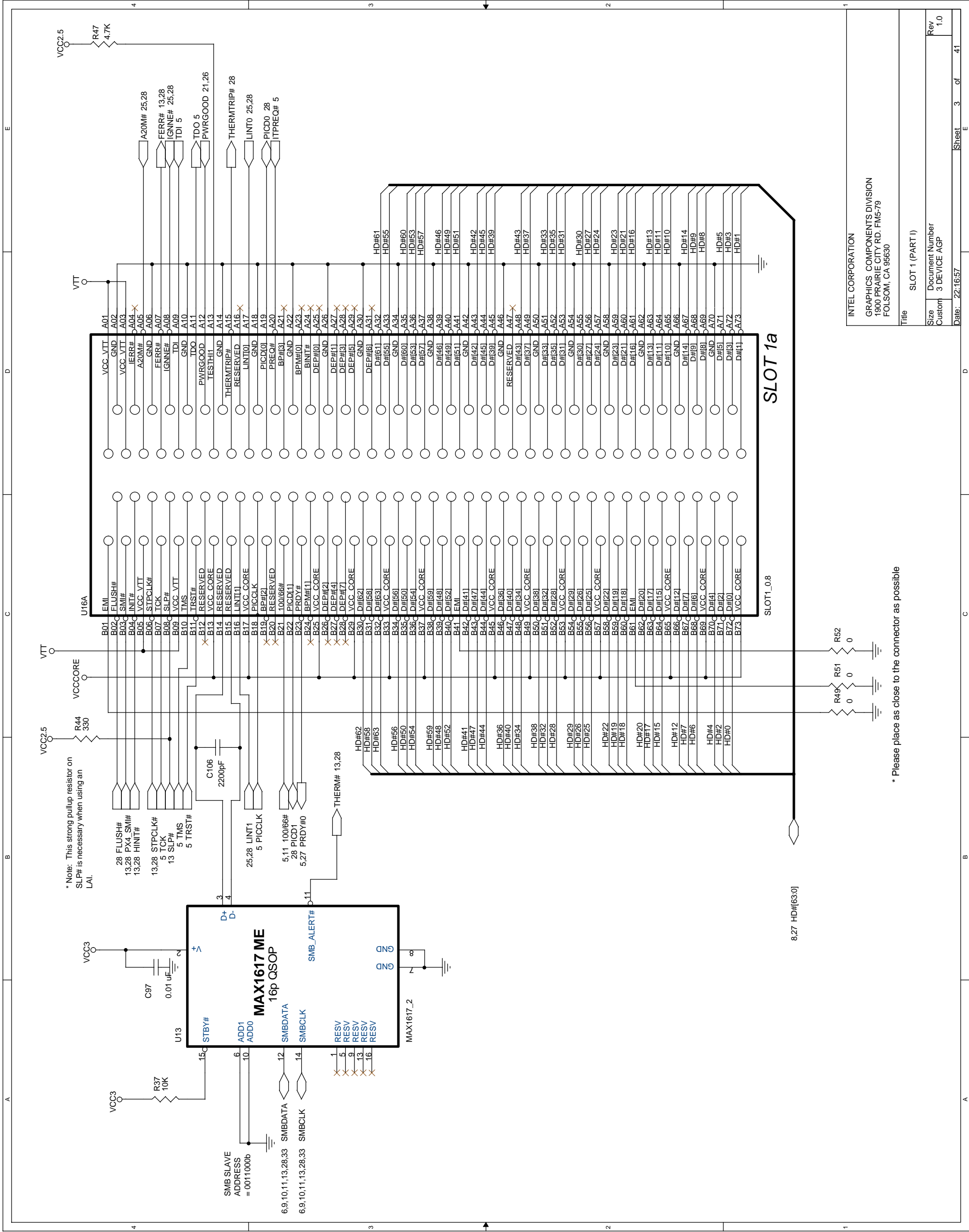


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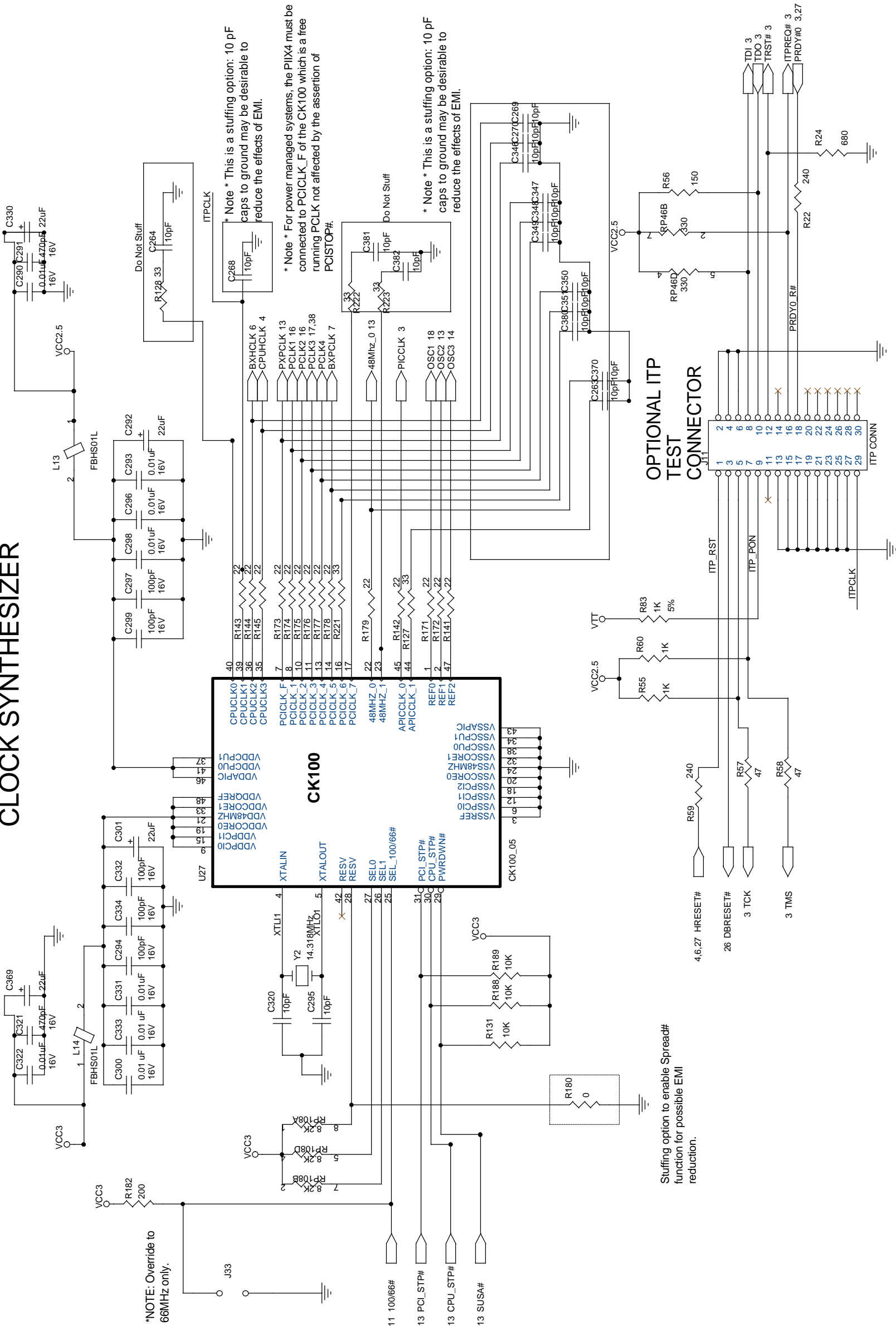
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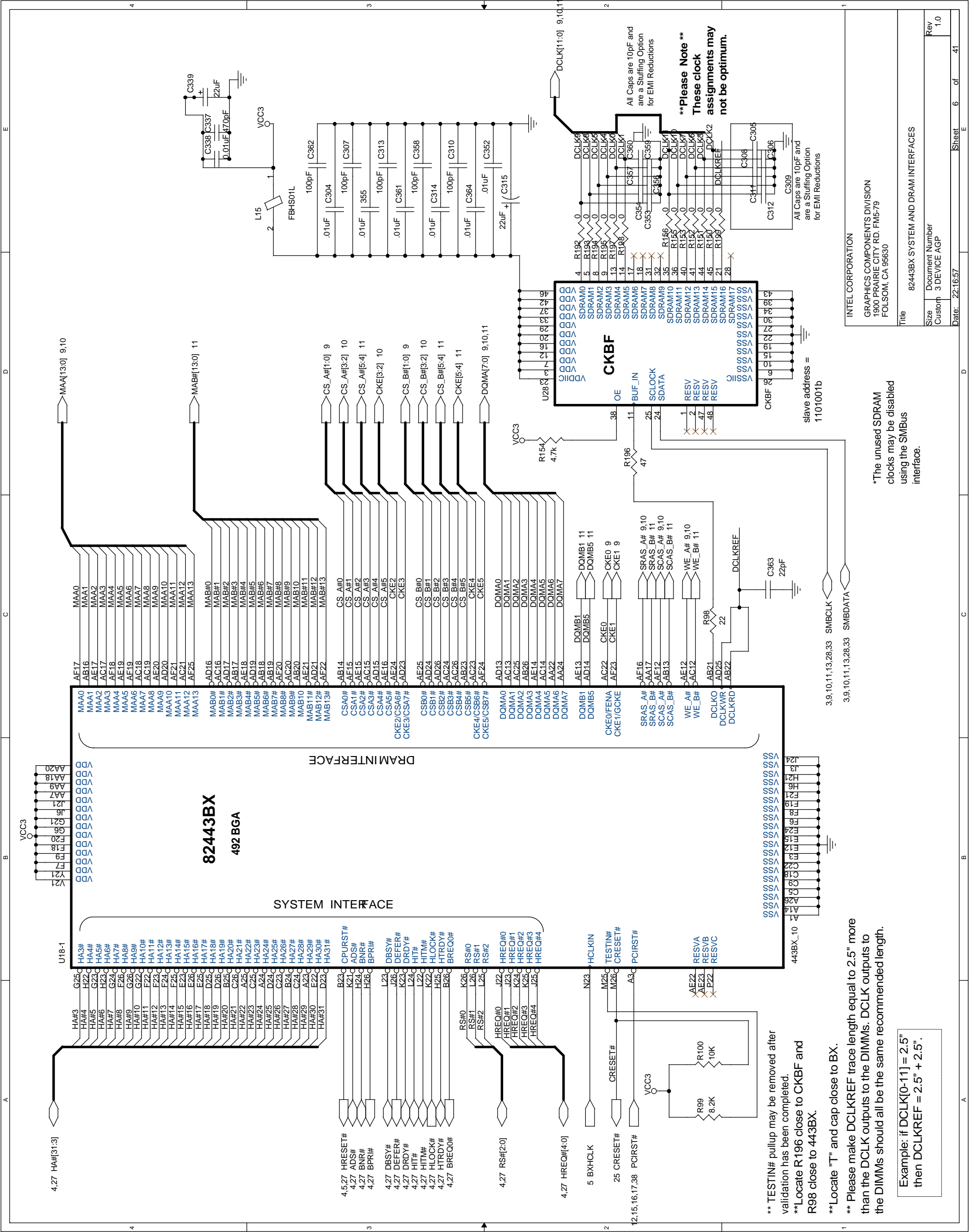
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Size	Document Number		Rev
	3 DEVICE AGP		
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CLOCK SYNTHESIZER





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Title 82443BX SYSTEM AND DRAM INTERFACES	
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*The unused SDRAM clocks may be disabled using the SMBus interface.

**Locate "T" and cap close to BX.

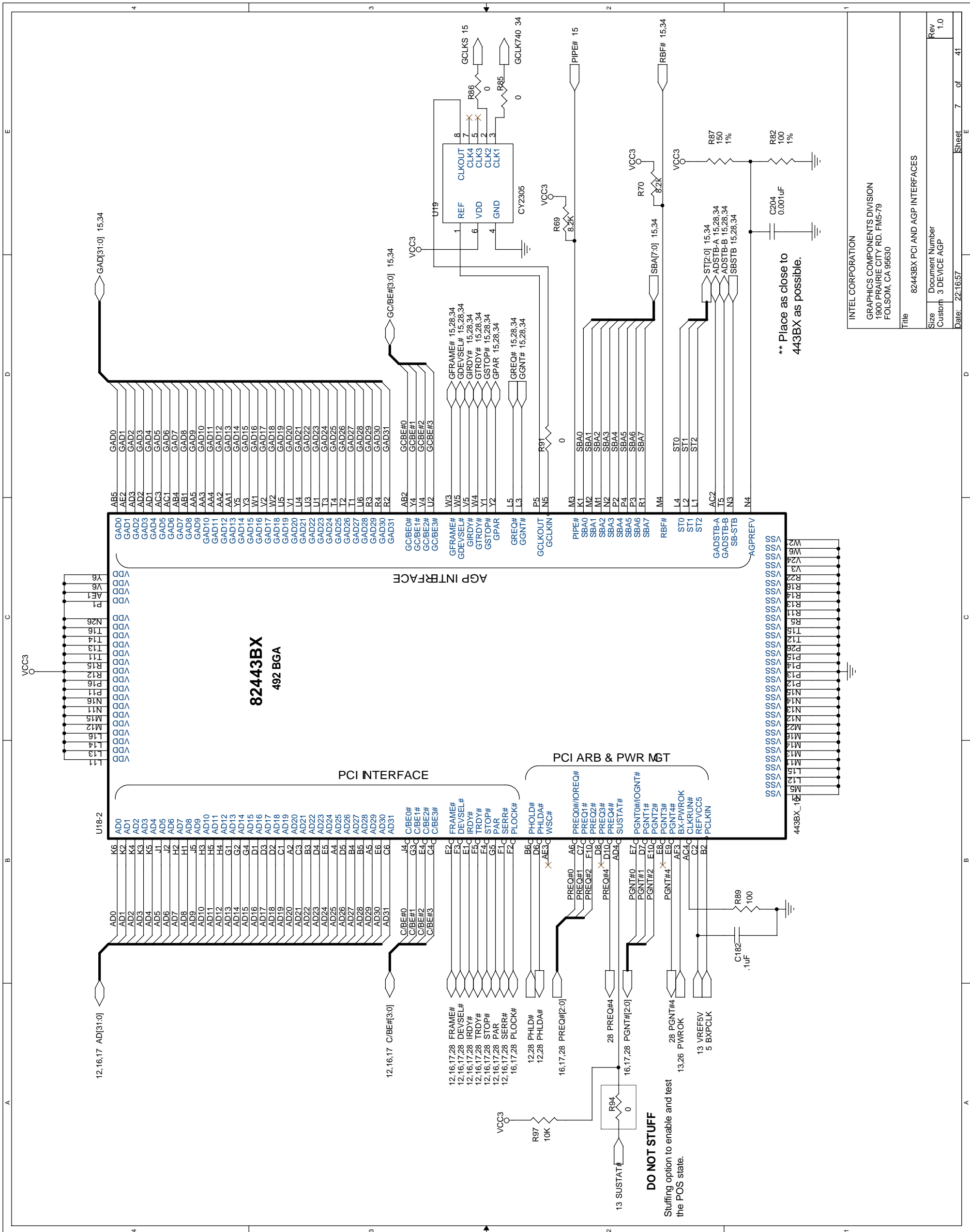
** TESTIN# pullup may be removed after validation has been completed.
**Locate R196 close to CKBF and R98 close to 443BX.

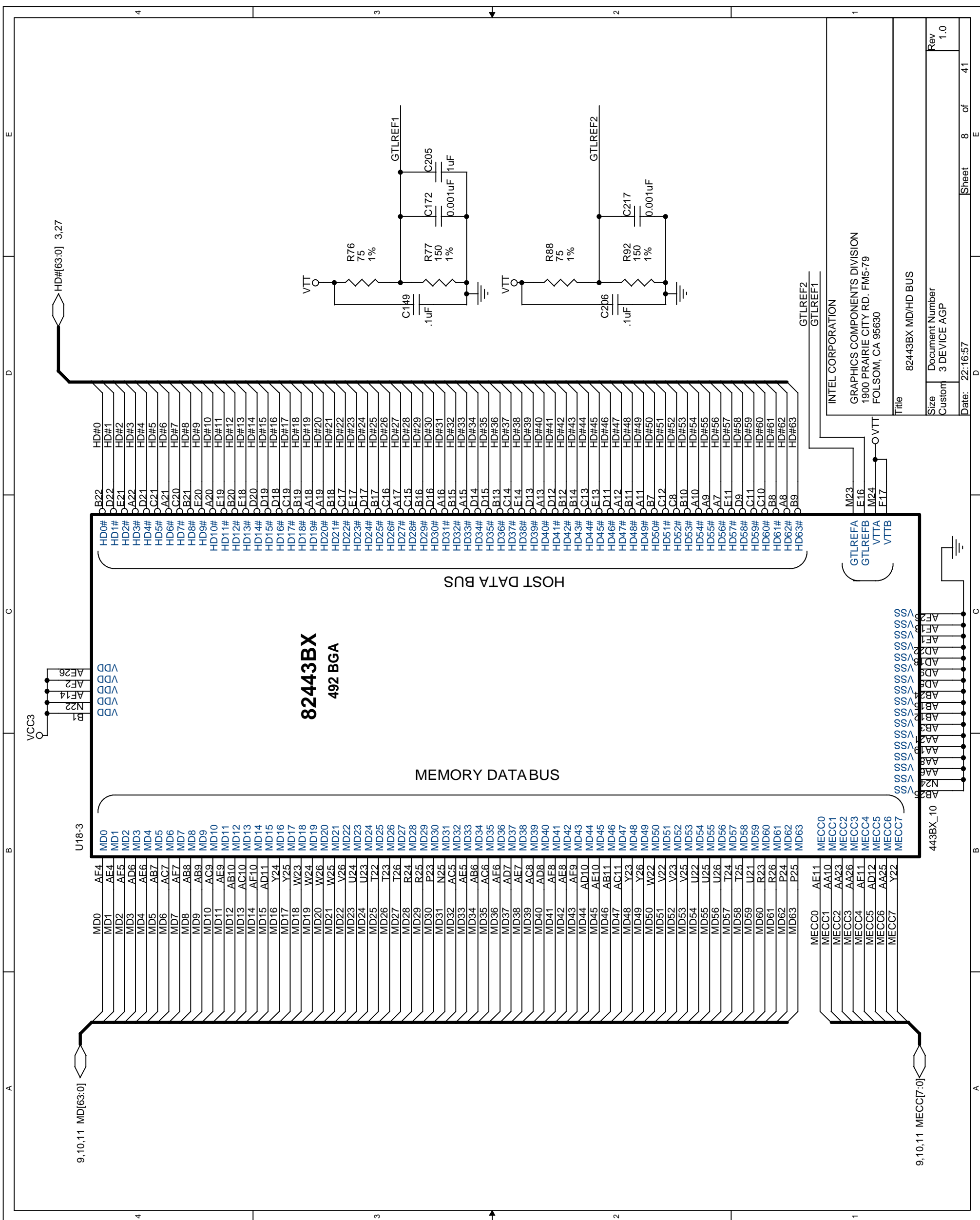
**Please Note **
These clock assignments may not be optimum.

All Caps are 10pF and are a Stuffing Option for EMI Reductions

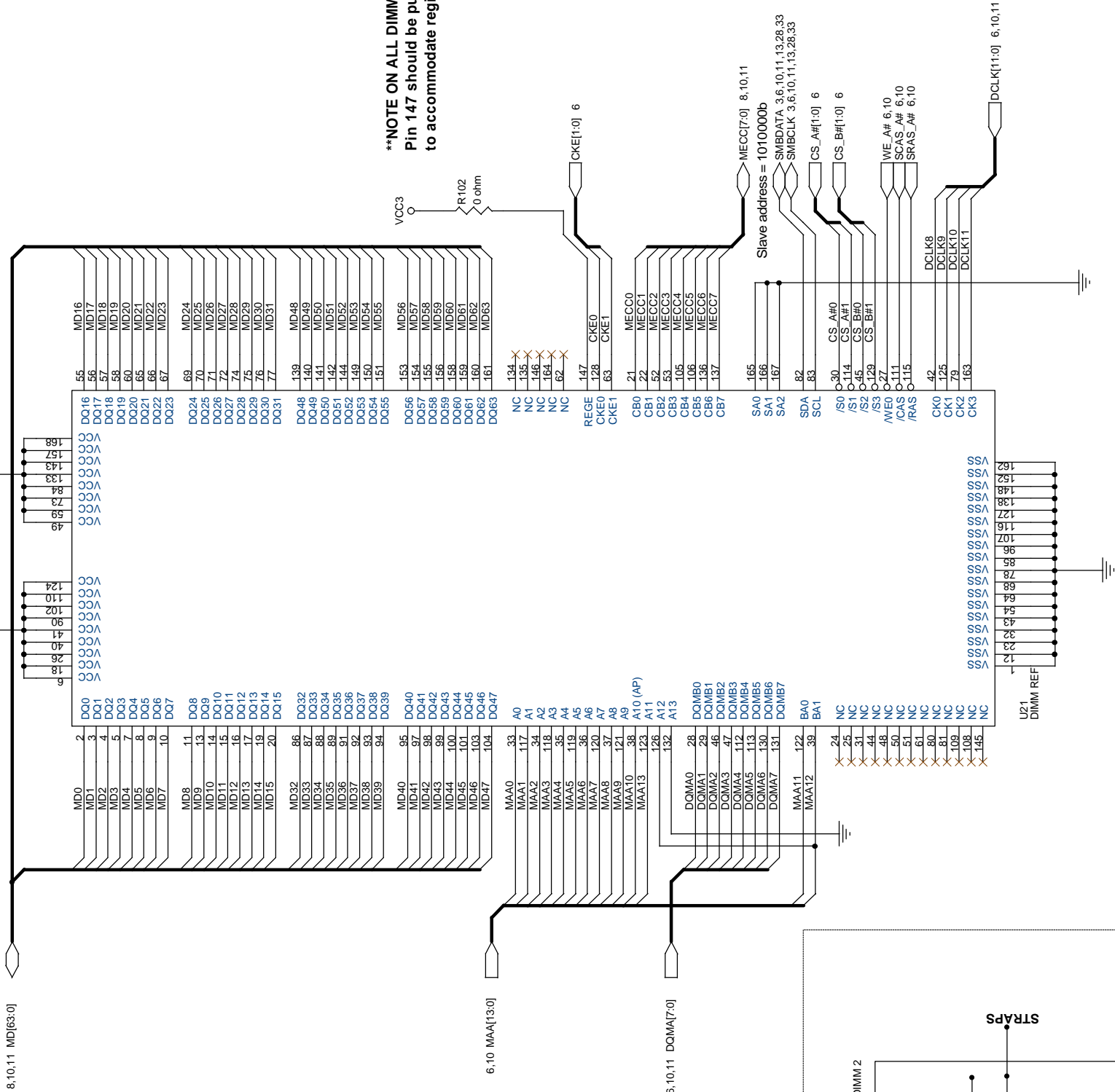
All Caps are 10pF and are a Stuffing Option for EMI Reductions

Example: if DCLK[0-11] = 2.5" then DCLKREF = 2.5" + 2.5".

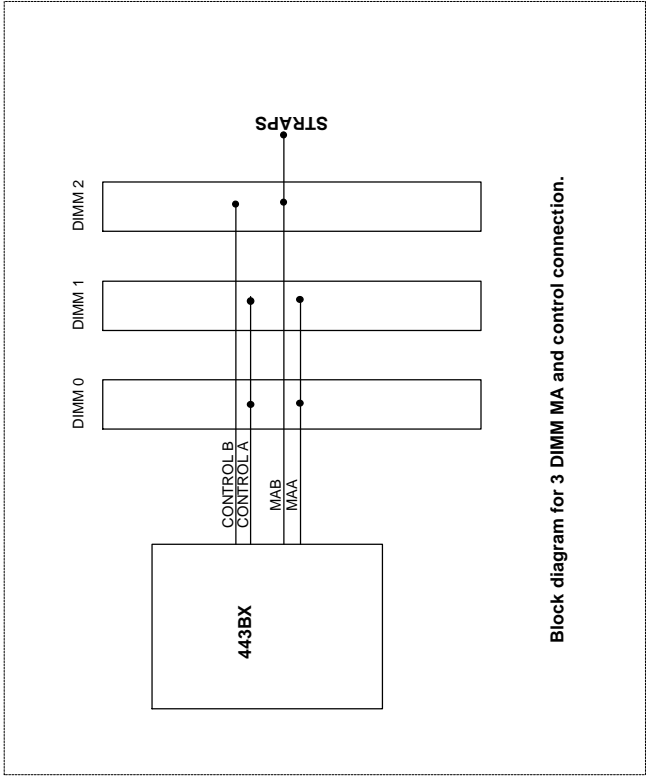




DIMM SOCKET 0

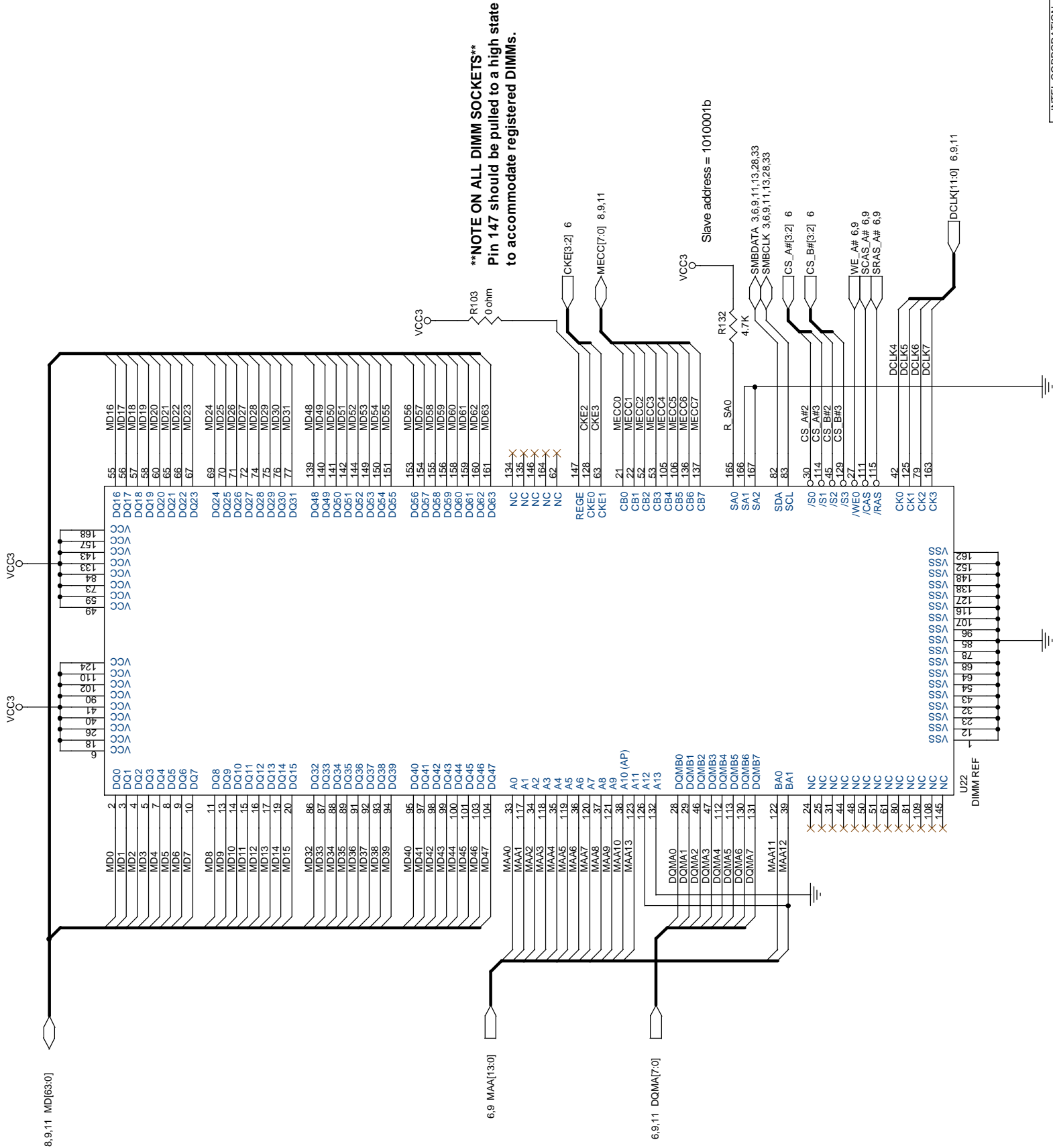


****NOTE ON ALL DIMM SOCKETS****
Pin 147 should be pulled to a high state
to accommodate registered DIMMs.



Block diagram for 3 DIMM MA and control connection.

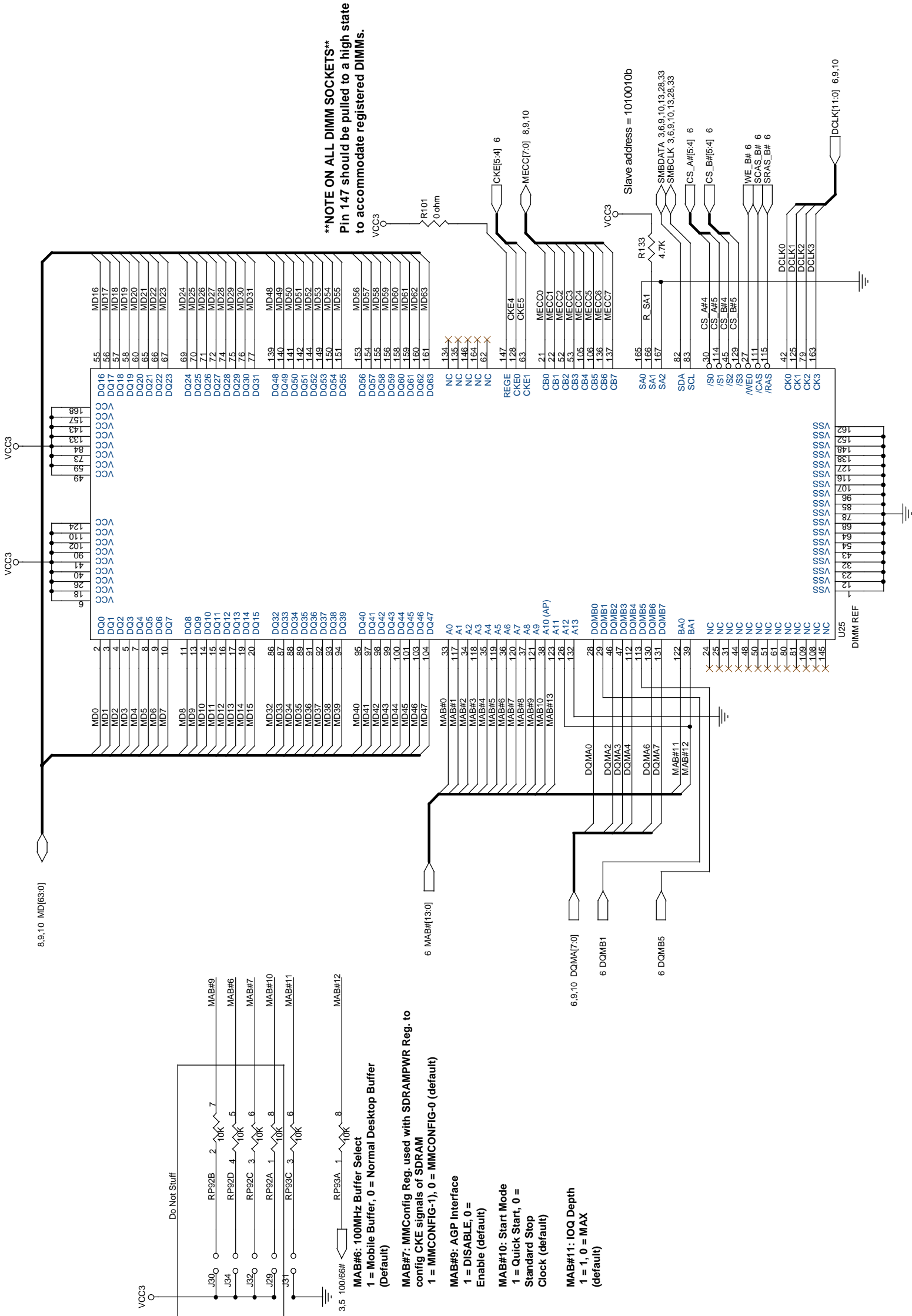
DIMM SOCKET 1



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Title		DIMM SOCKET 1	
Size	Document Number		3 DEVICE AGP
	Custom		
Date: 22:16:57			

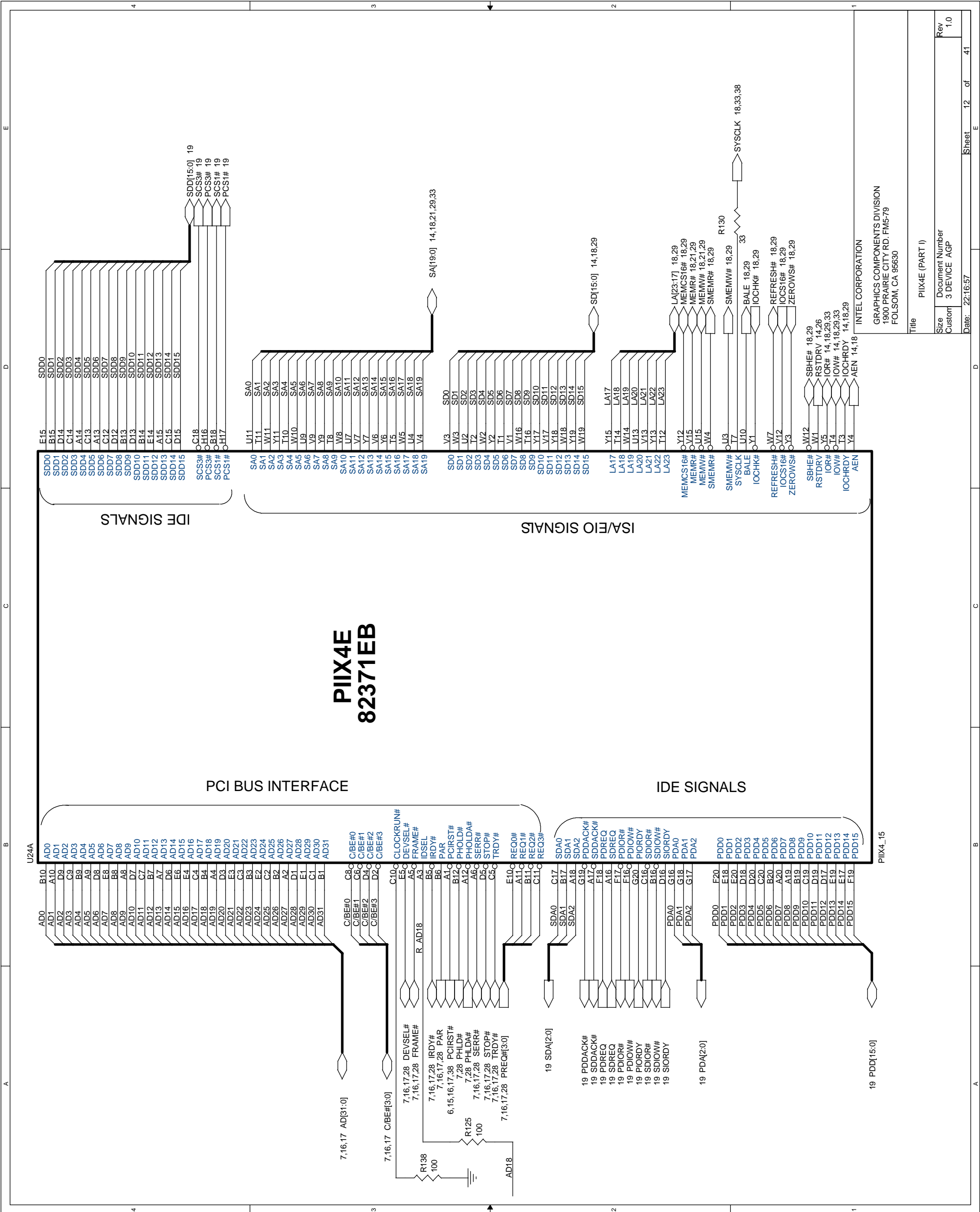
DIMM SOCKET 2

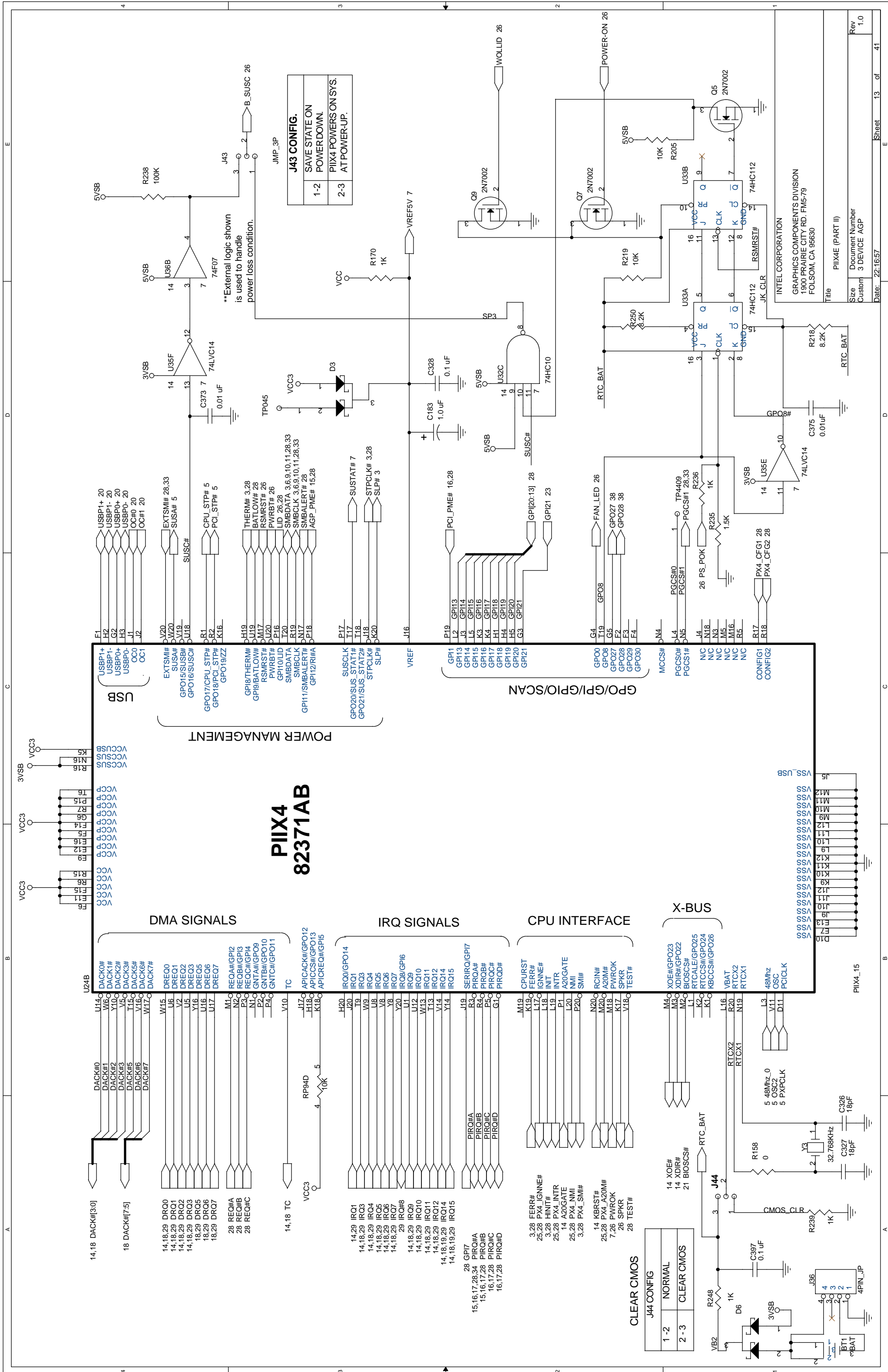


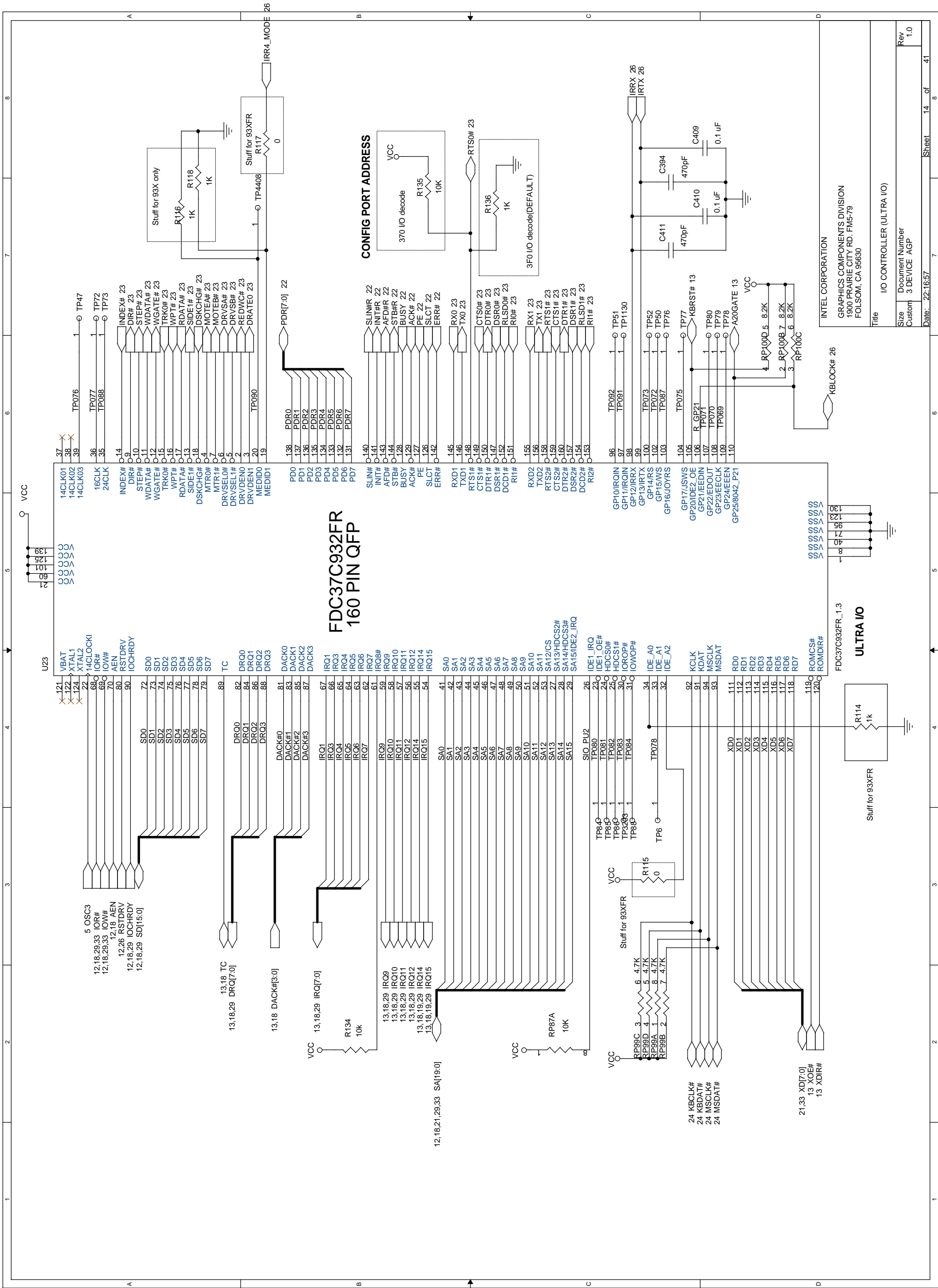
****NOTE ON ALL DIMM SOCKETS****
Pin 147 should be pulled to a high state
to accommodate registered DIMMs.

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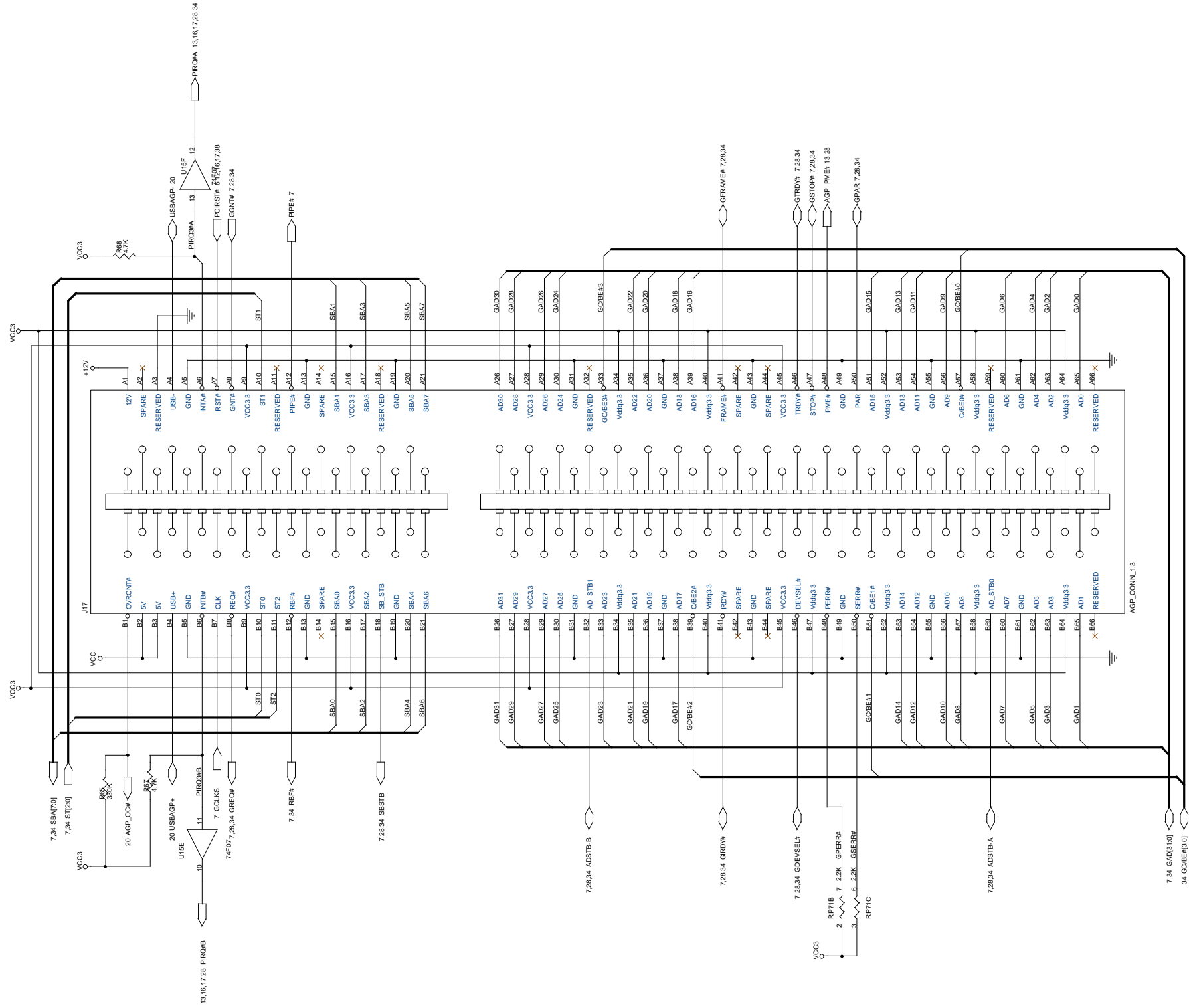
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AGP CONNECTOR



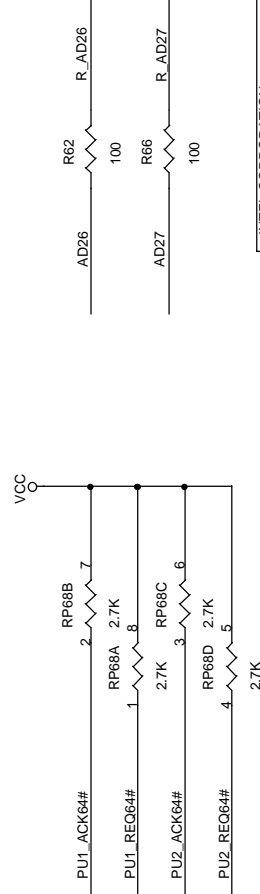
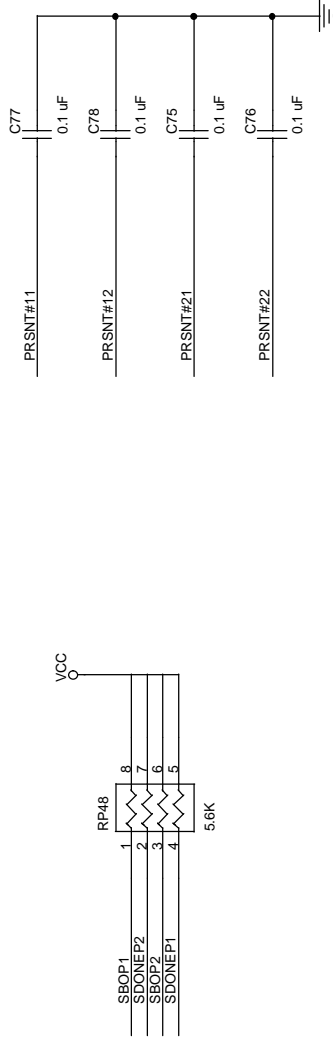
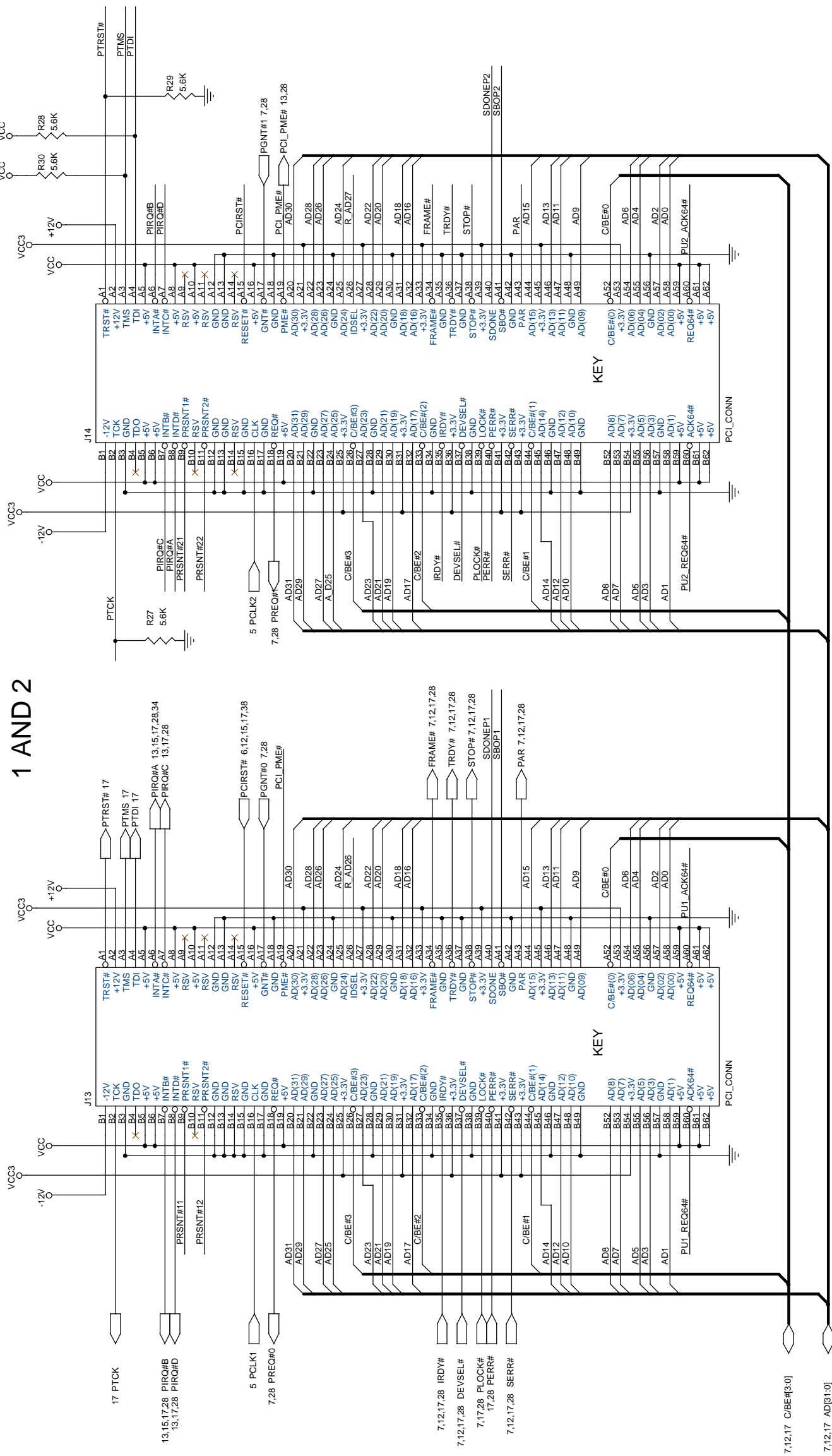
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Title
ACCELERATED GRAPHICS PORT (AGP) CONNECTOR

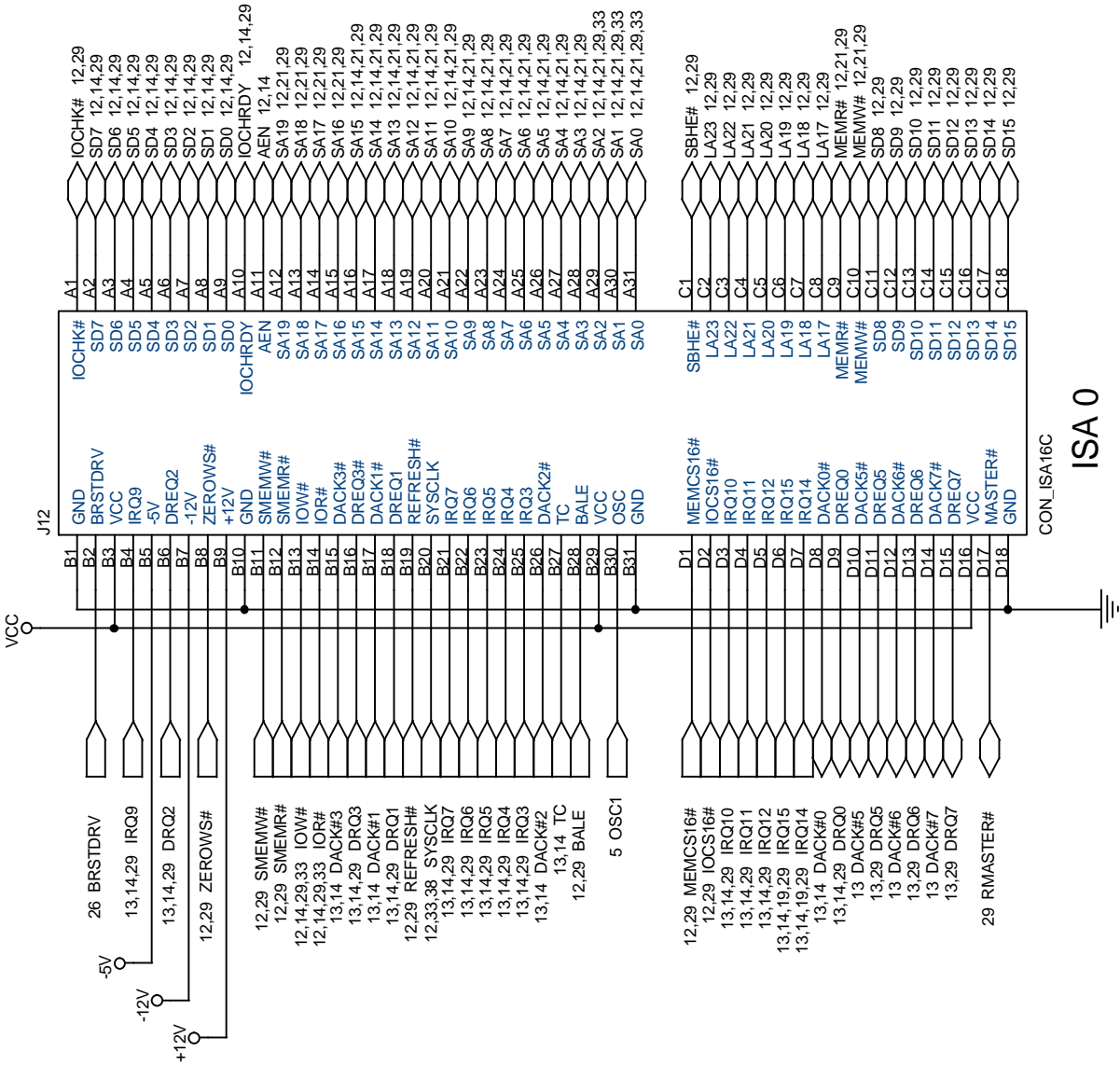
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PCI CONNECTORS 1 AND 2

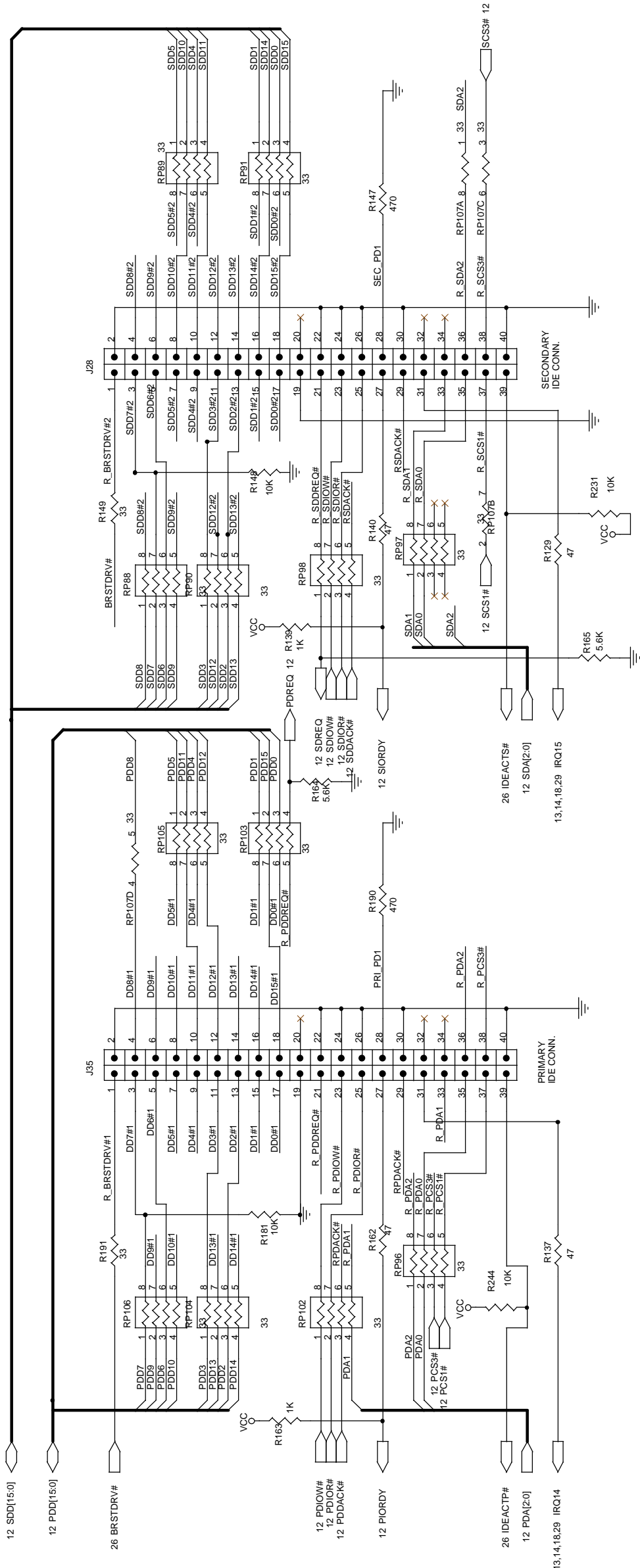


ISA SLOTS

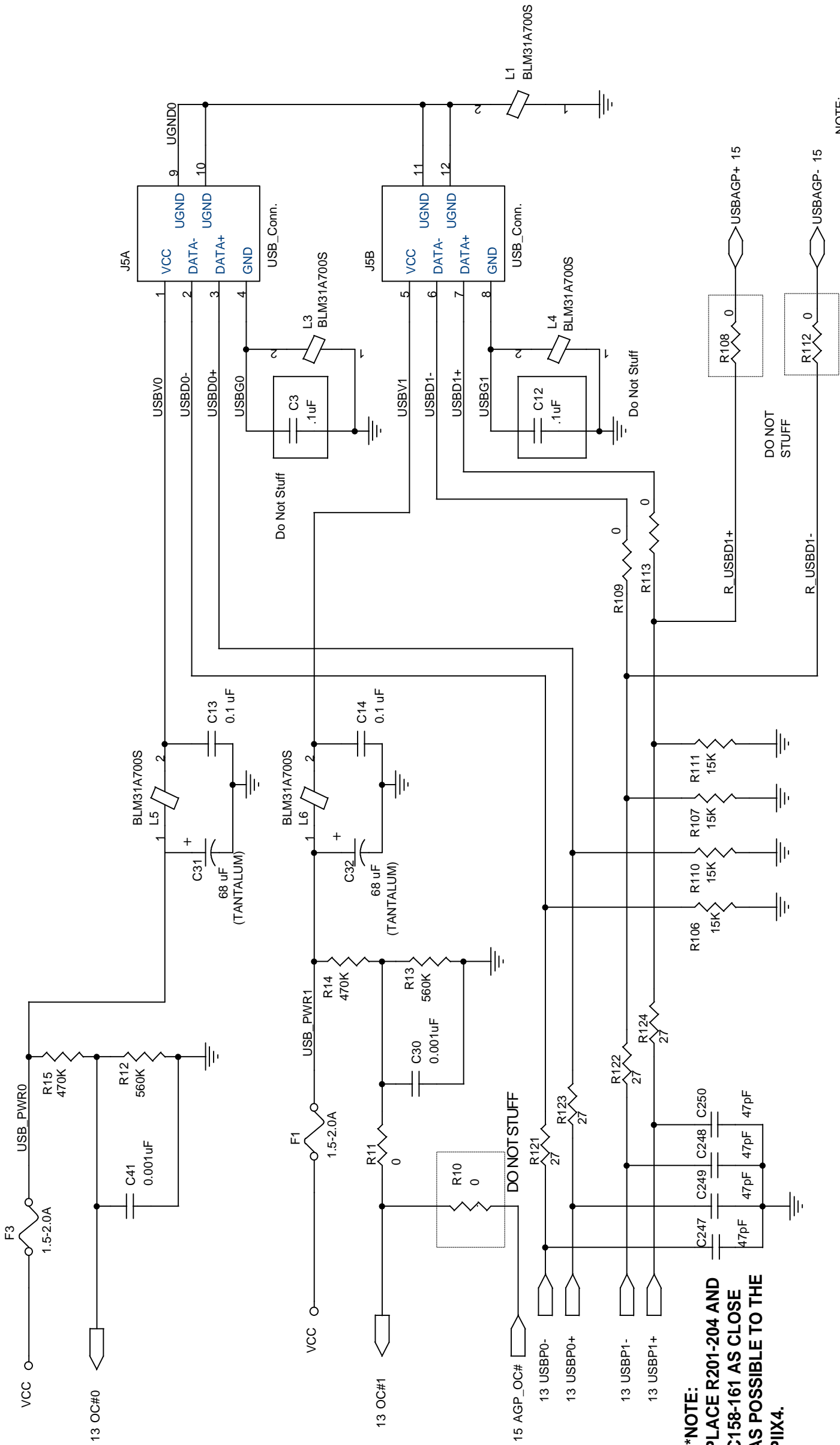


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TitleISA SLOTS			
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IDE CONNECTORS



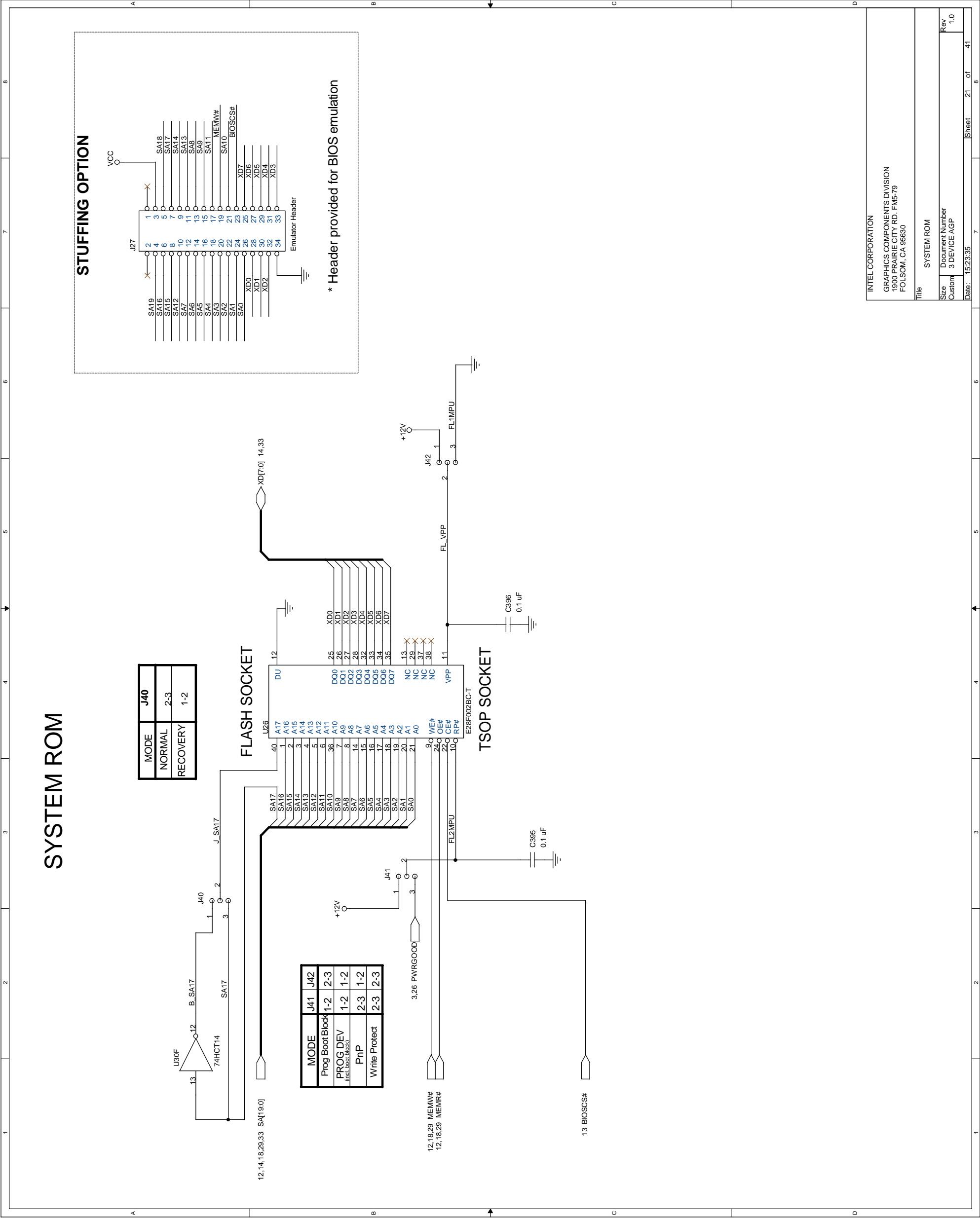
USB CONNECTORS

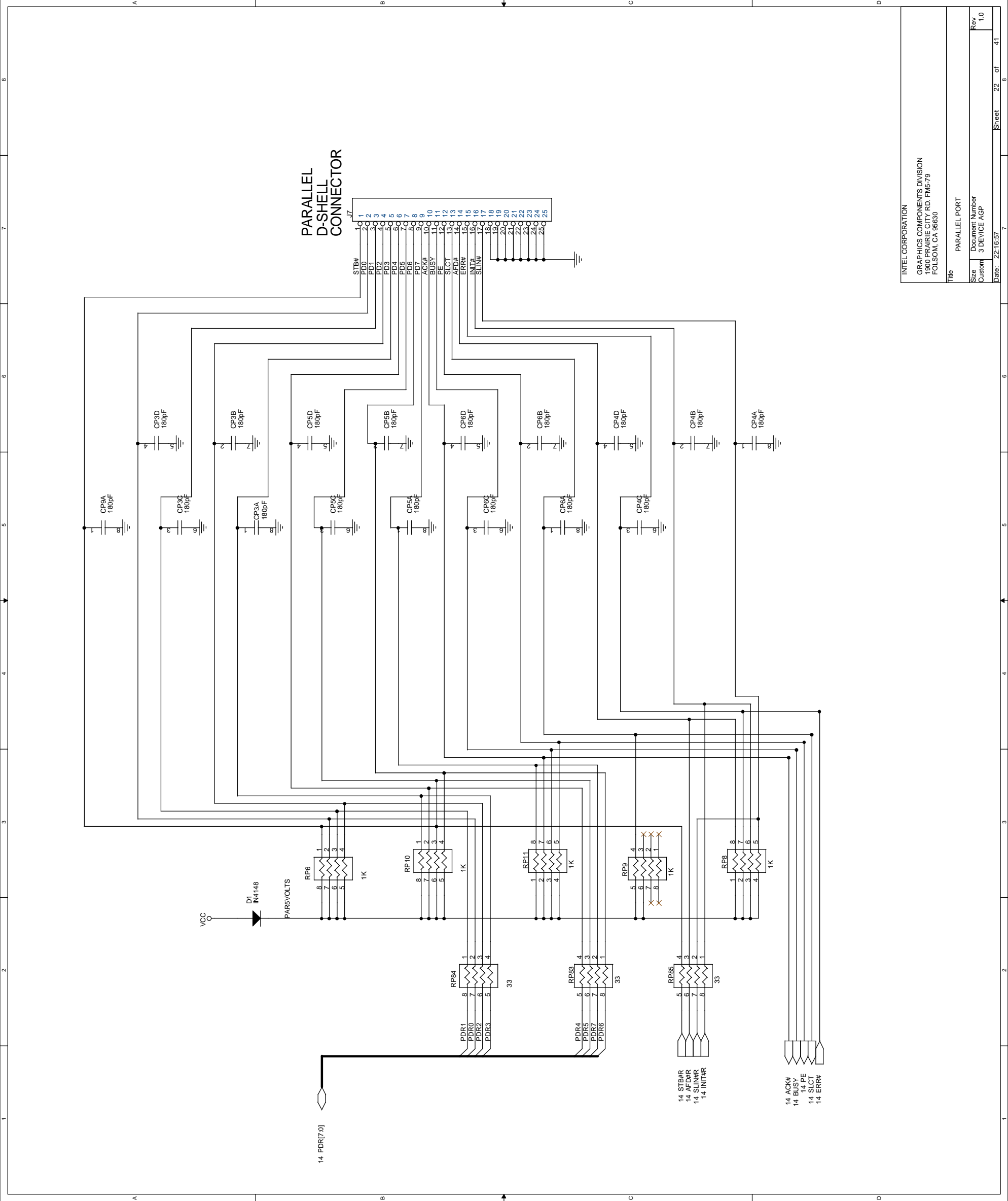


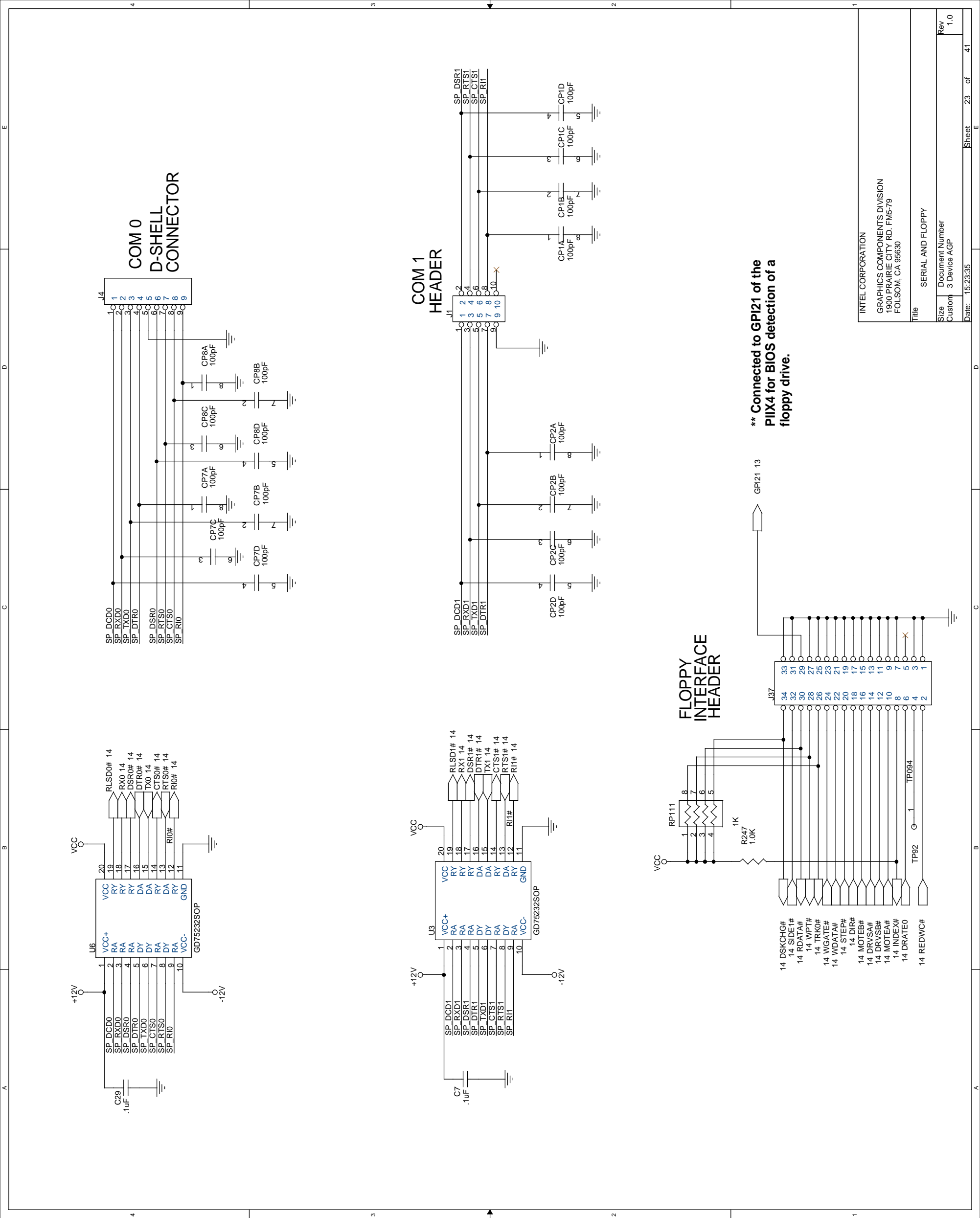
****NOTE:**
PLACE R201-204 AND
C158-161 AS CLOSE
AS POSSIBLE TO THE
PIIX4.

NOTE:
USE PIIX4
APPLICATION NOTE
FOR LAYOUT
GUIDELINES

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Title SERIAL AND FLOPPY		
Size	Document Number	Rev
Custom	3 Device AGP	1.0
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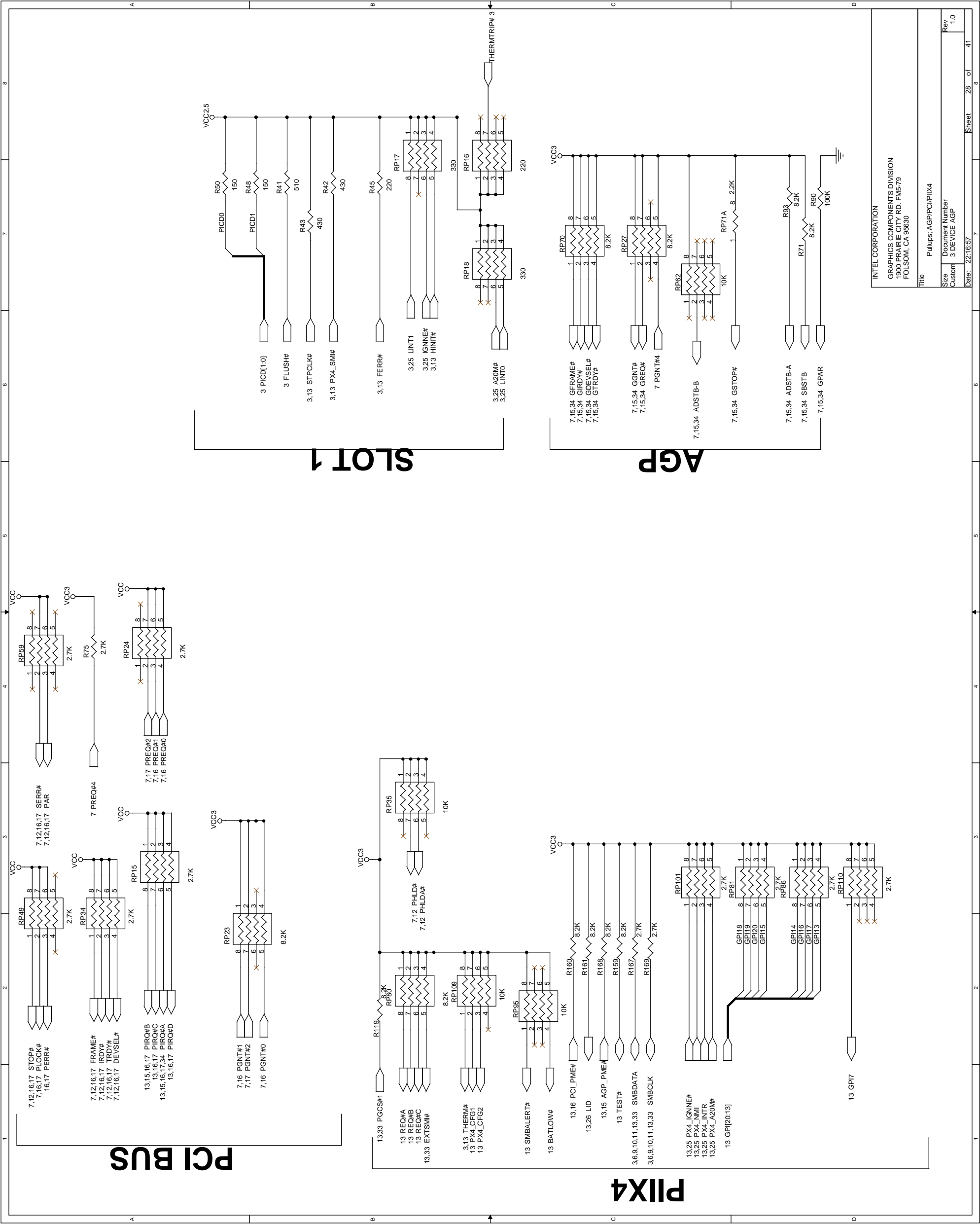
Title		KEYBOARD/MOUSE INTERFACE	Rev 1.0
Size Custom	Document Number 3 DEVICE AGP		
Date: 22:16:57	Sheet 24 of 41		

*NOTE: May be removed if route lengths can be restricted to 1.5" MIN to 4.0" MAX.

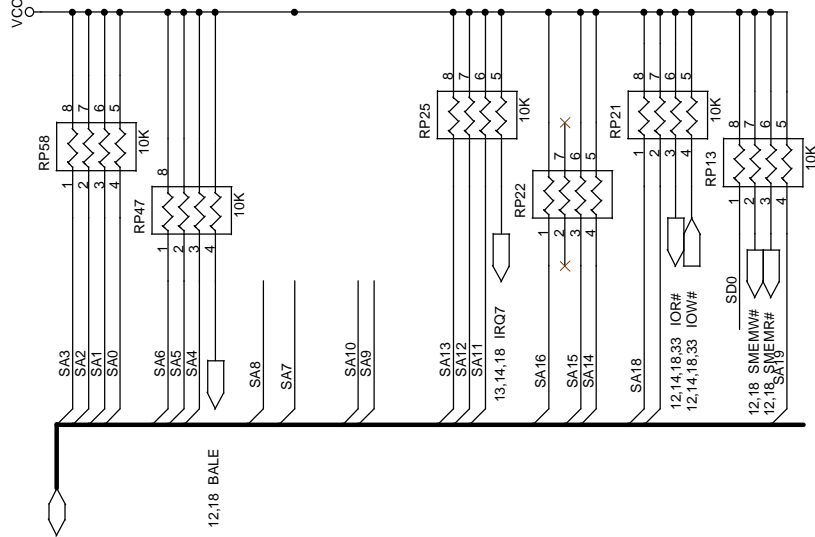
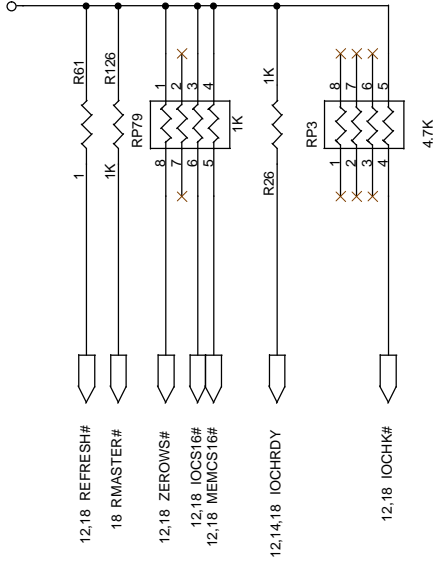
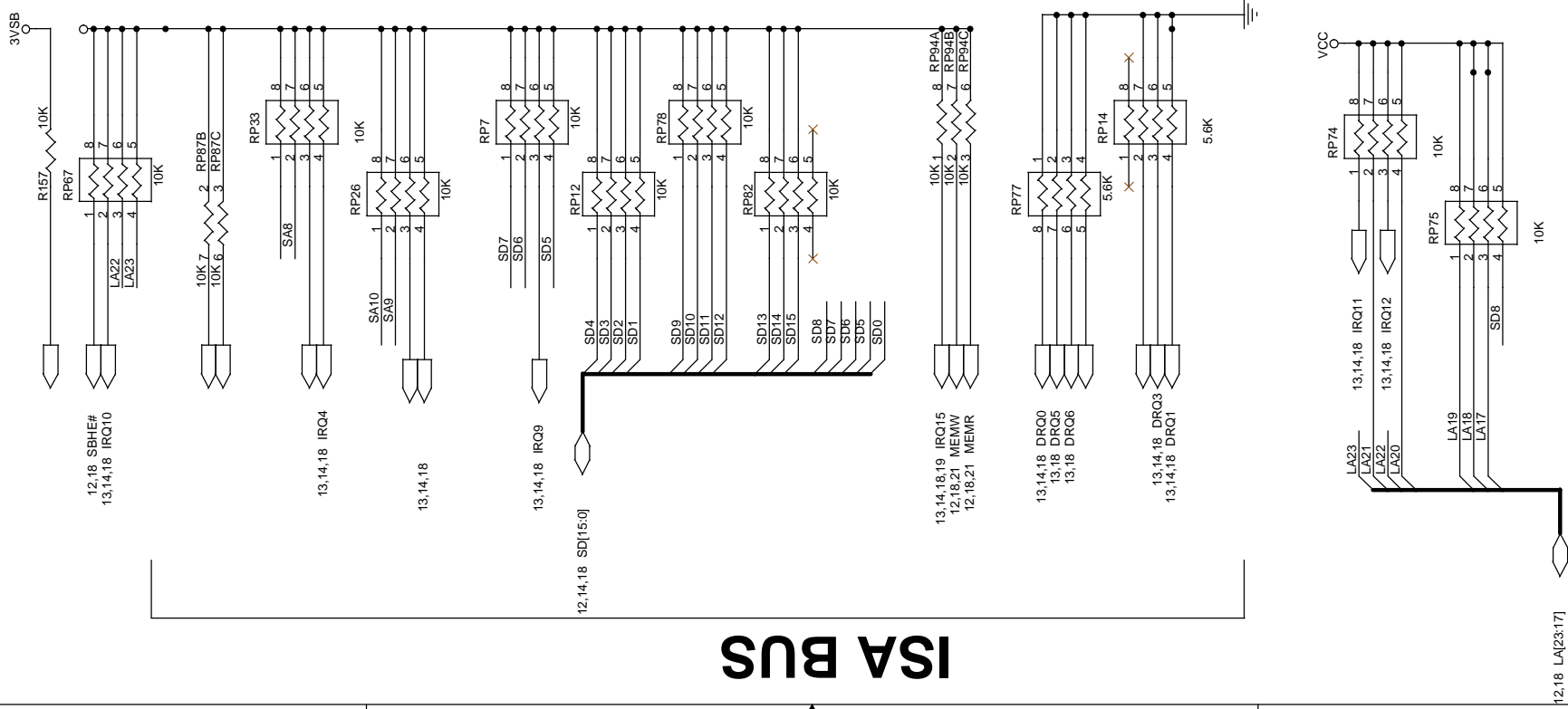


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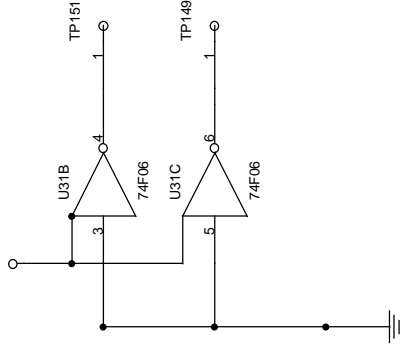
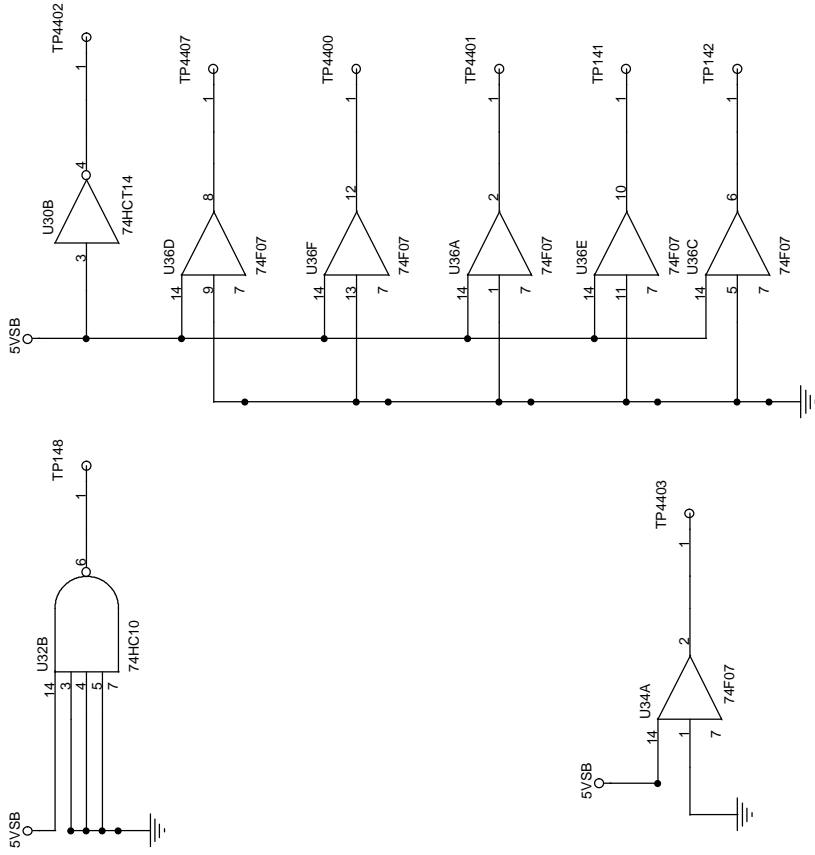
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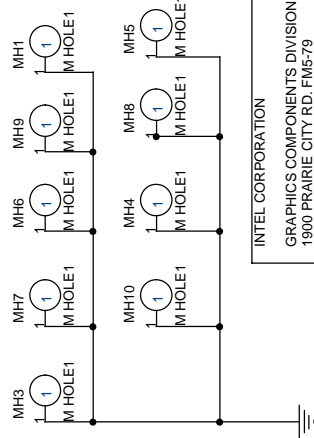
ISA BUS



UNUSED GATES

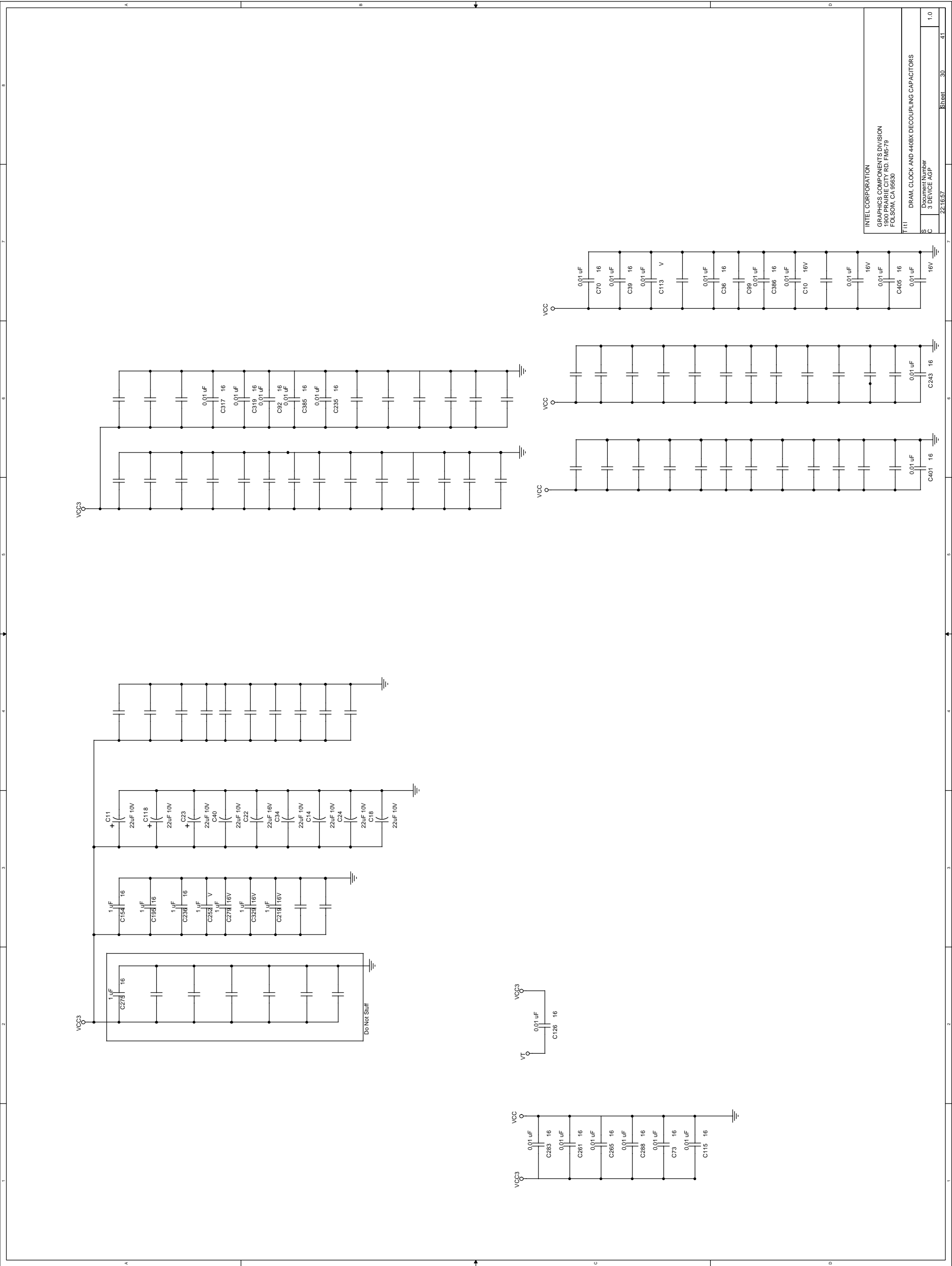


Mounting Holes

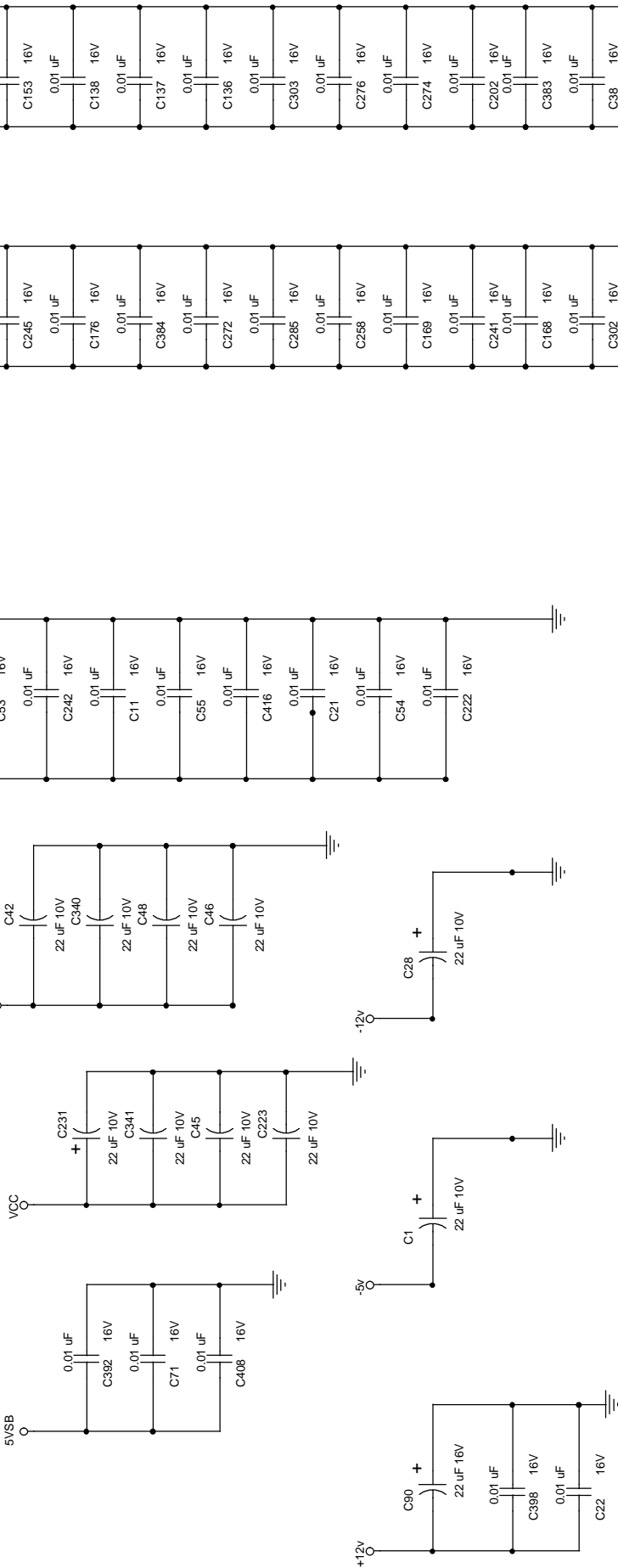


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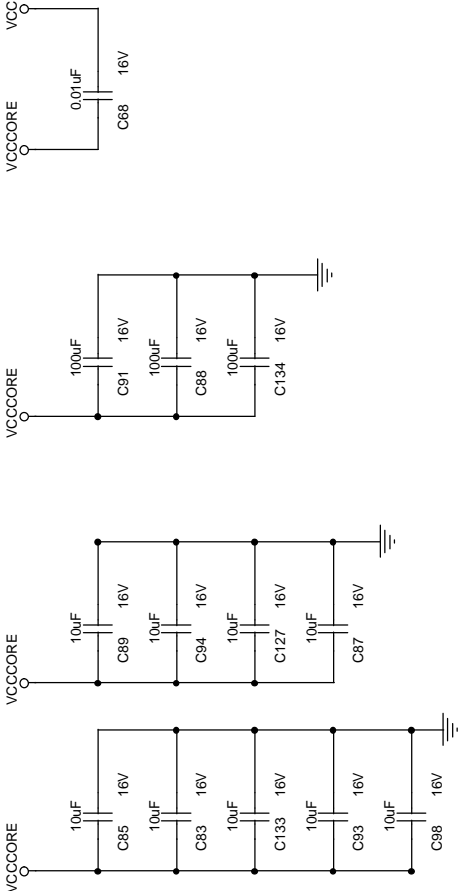
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Size	Custom	Document Number	3 DEVICE AGP		
Date:		Sheet	29	of	41



BULK POWER DECOUPLING



CORE VOLTAGE DECOUPLING



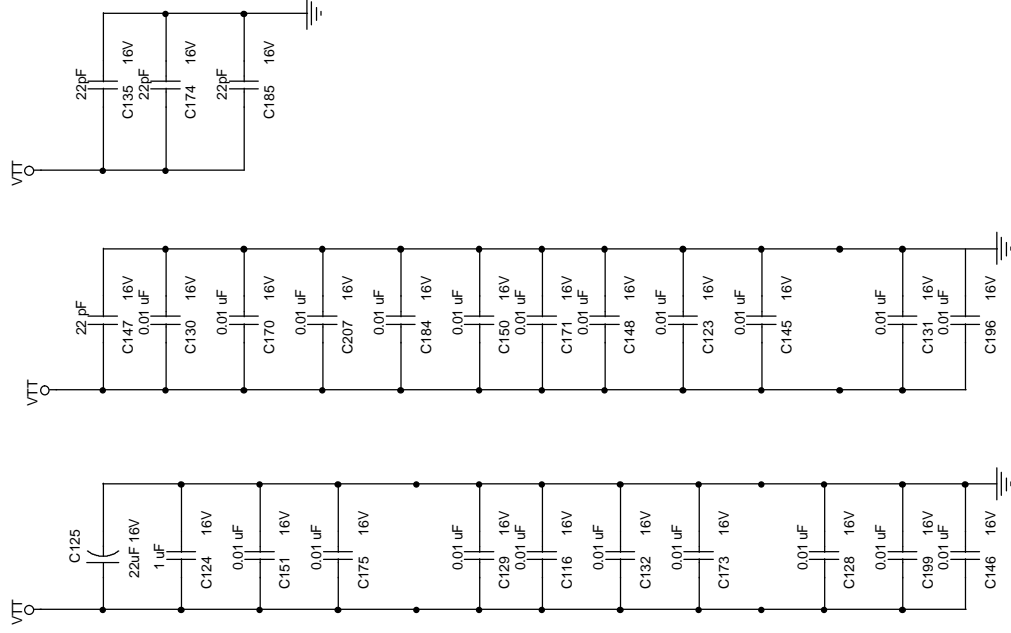
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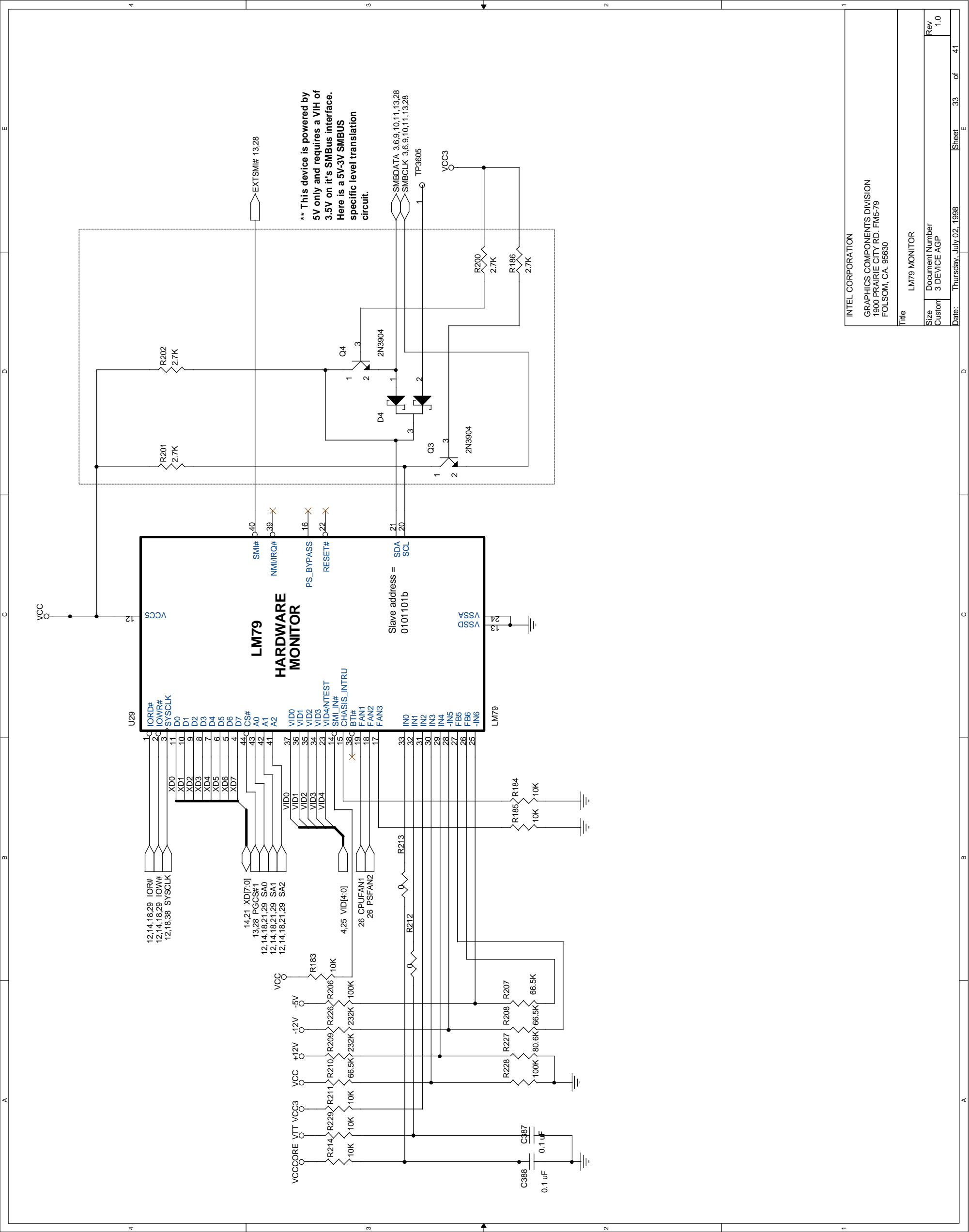
Title 3.3 VOLT AND BULK POWER DECOUPLING

Size	Document Number	Rev
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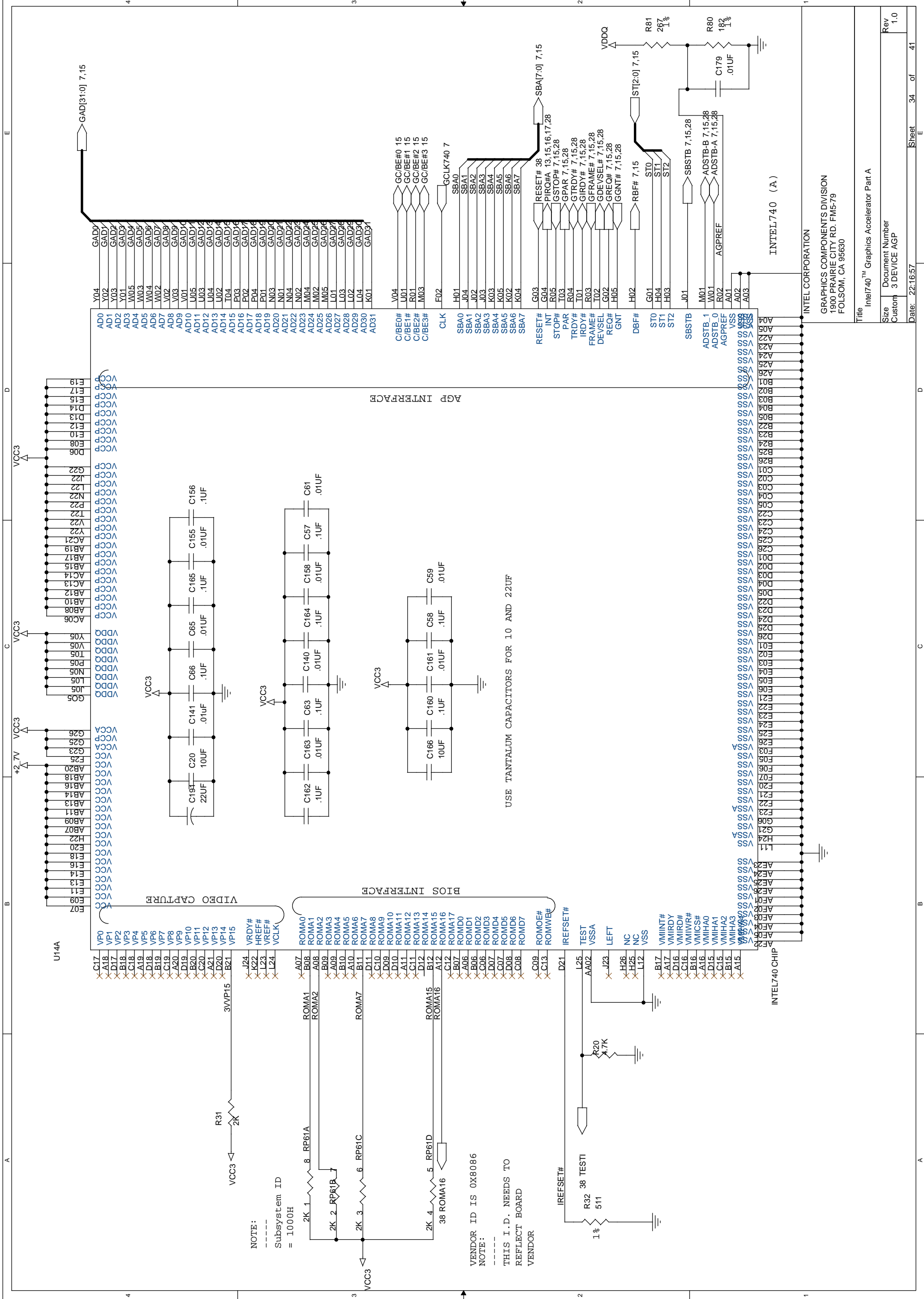
TERMINATION VOLTAGE DECOUPLING

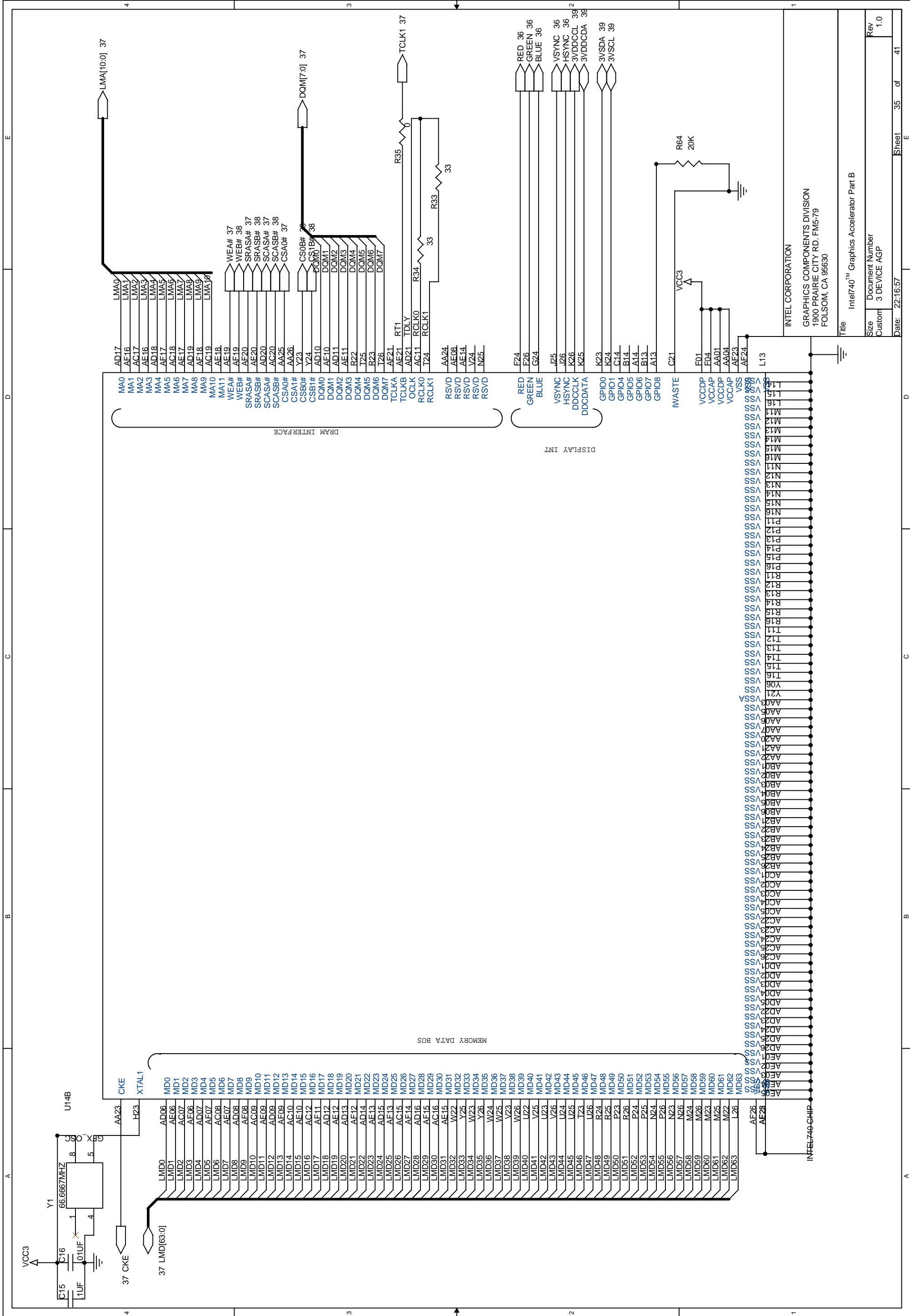


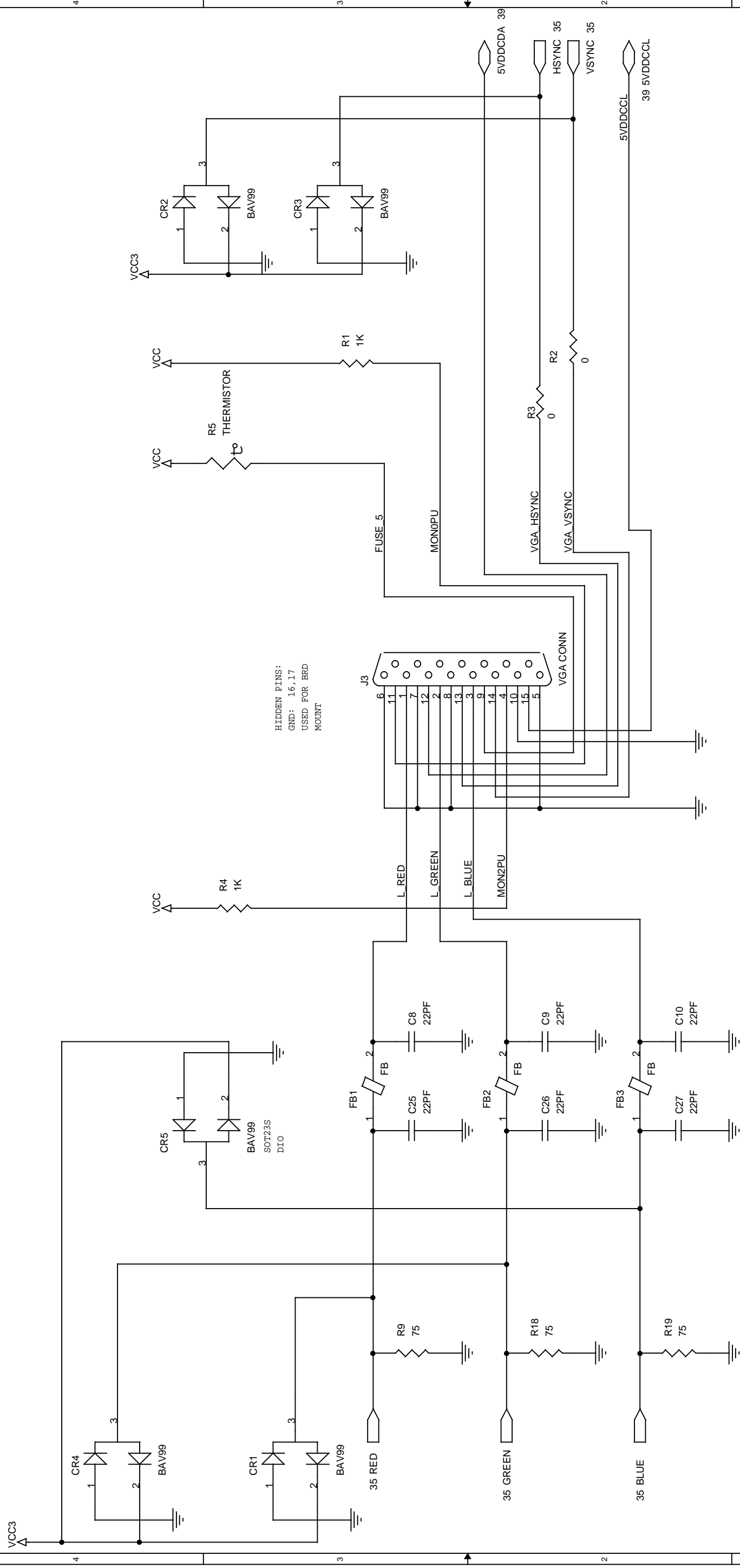


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Title		LM79 MONITOR	
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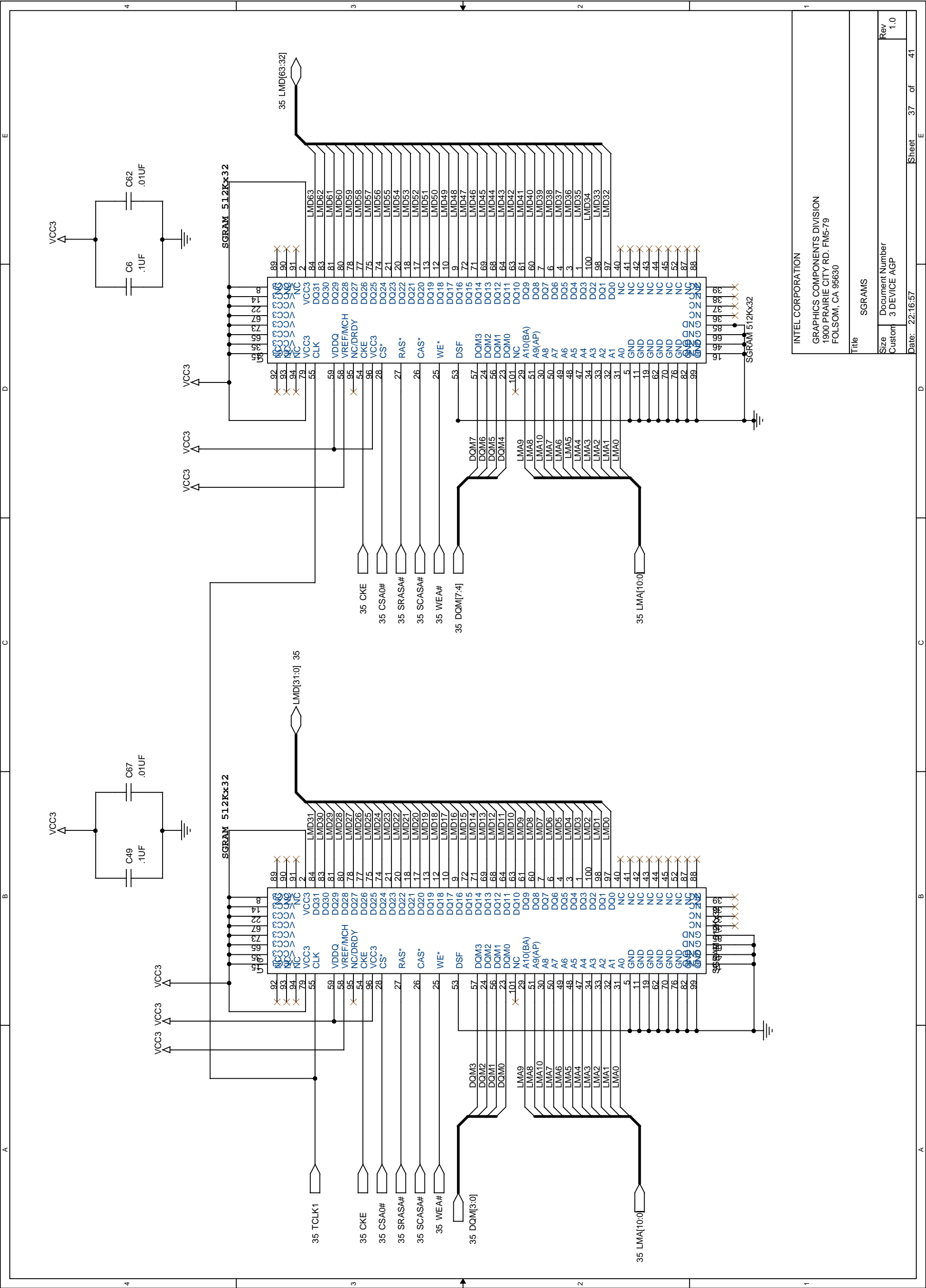


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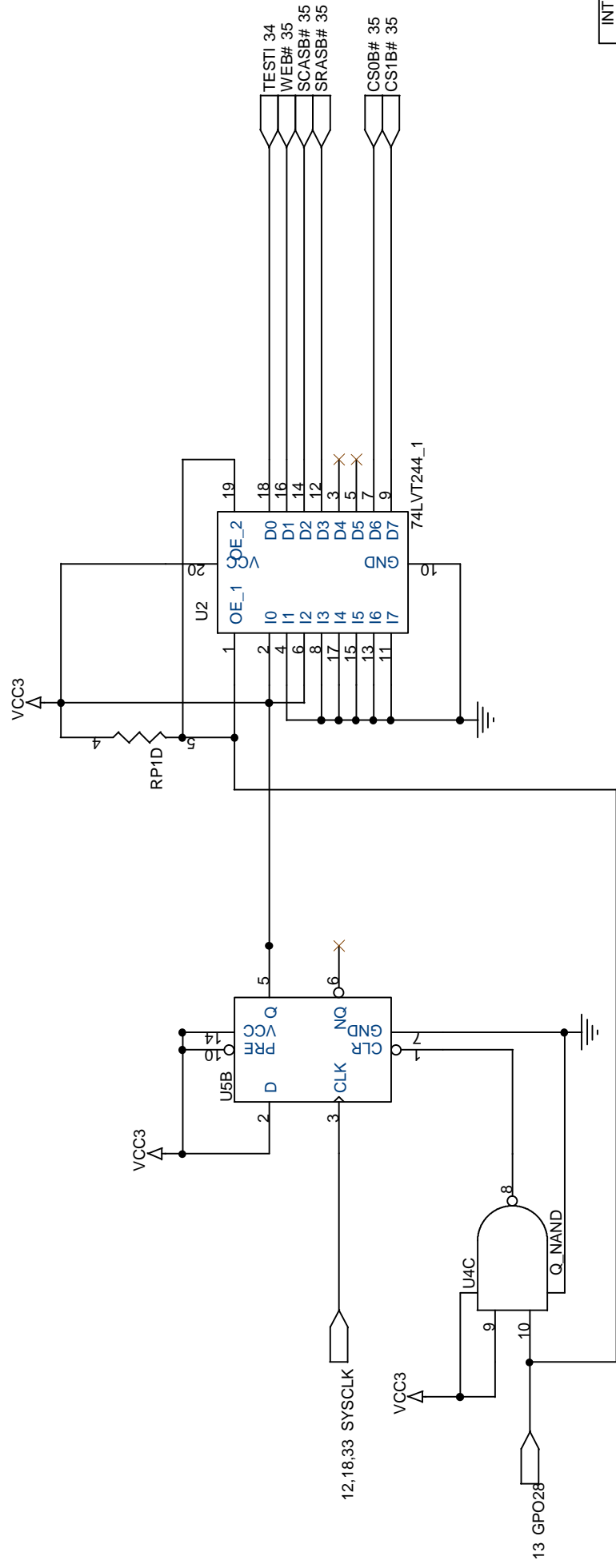
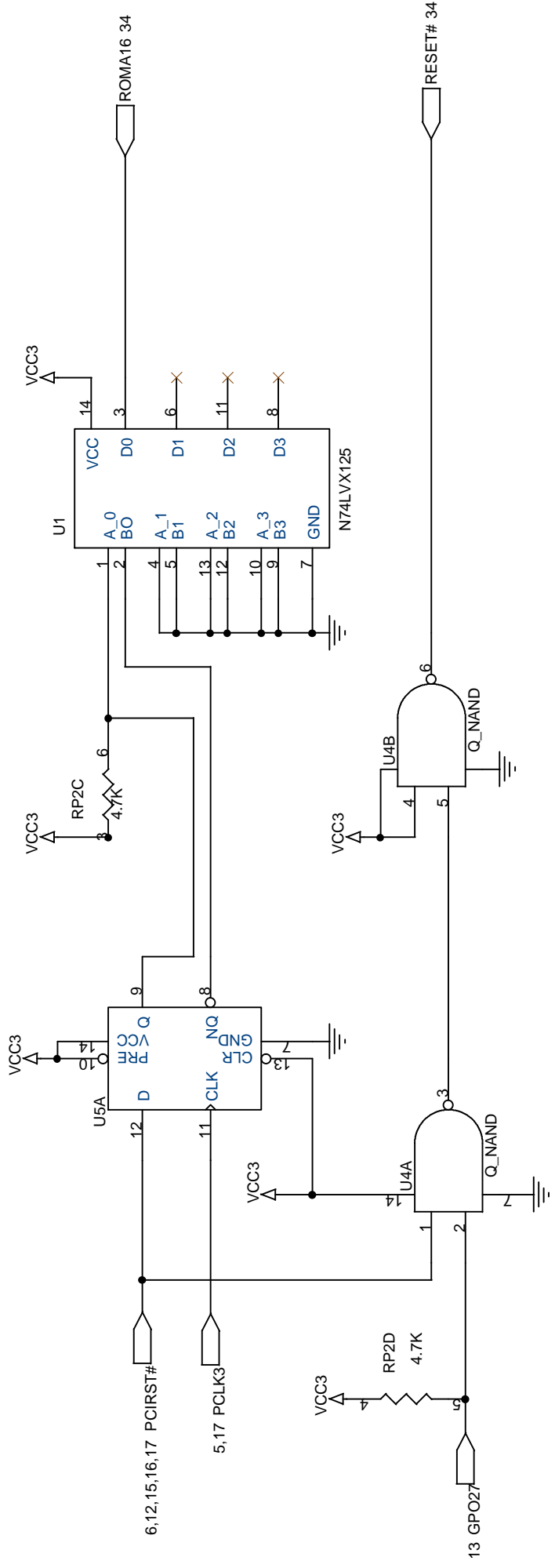
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VGA CONNECTOR

Size	Document Number	Rev
Custom	3 DEVICE AGP	1.0

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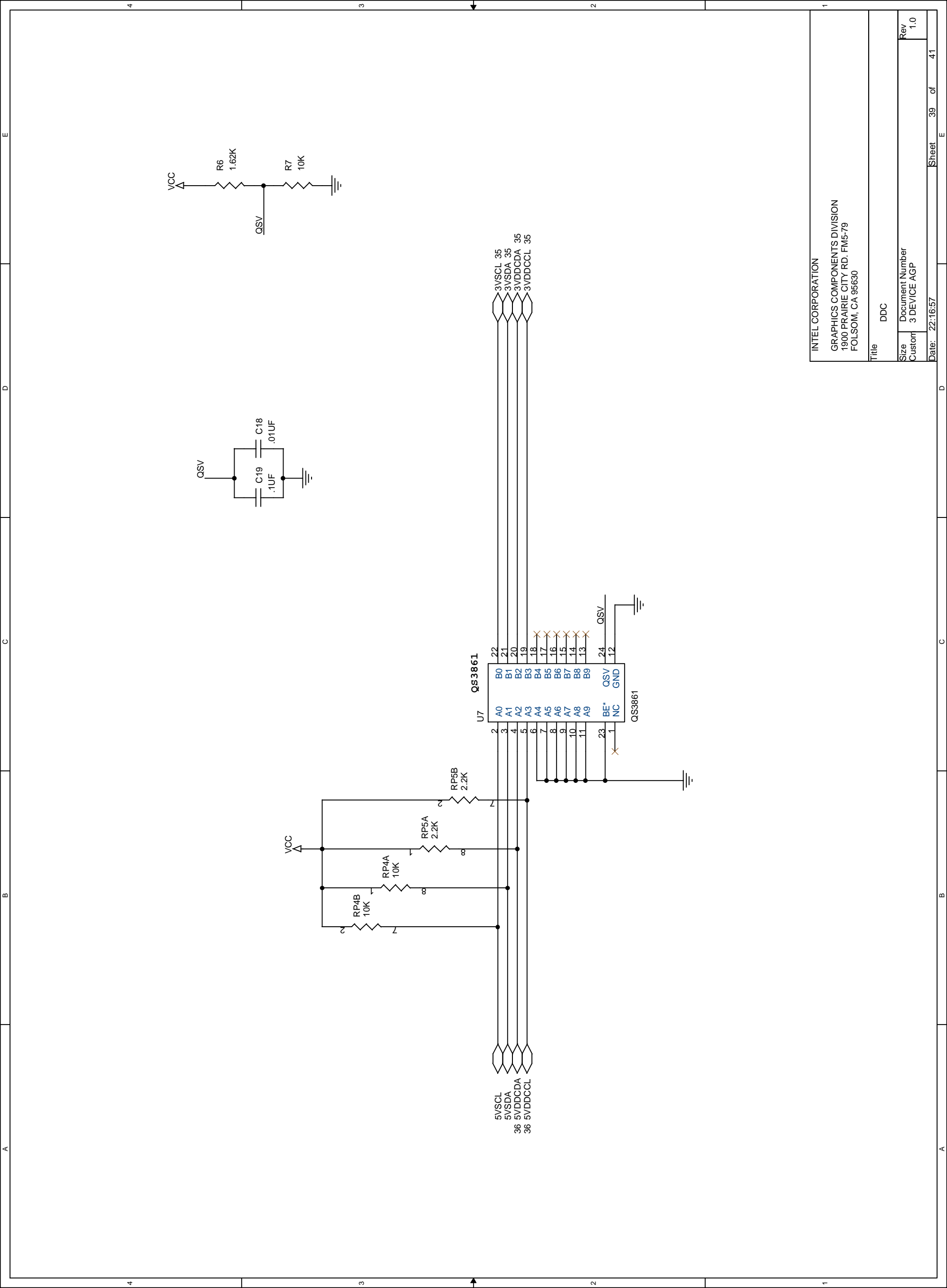


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Title SGRAMS		
Size Custom	Document Number 3 DEVICE AGP	Rev 1.0
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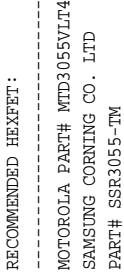


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Title			
LOW POWER MODE LOGIC			
Size Custom	Document Number 3 DEVICE AGP	Rev 1.0	
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Title DDC	
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Title VOLTAGE REGULATOR	
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REVISION1.0 8/98 -First release of 3 Device AGP schematics.

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Title REVISION HISTORY

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